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3D INTEGRATION, A SMART WAY TO ENHANCE PERFORMANCE

Leti Devices Workshop | December 3, 2017

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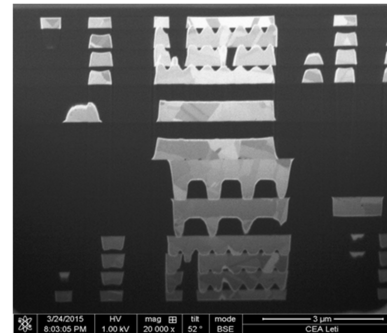
OVERAL GOAL OF THIS TALK

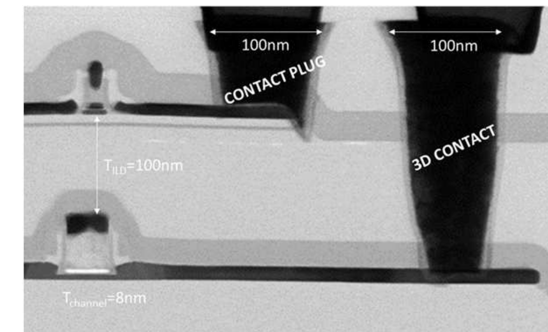
3D VLSI technologies

(3D VIA Pitch <5µm)

Hybrid bonding

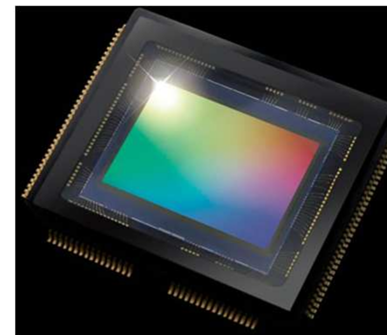


3D sequential

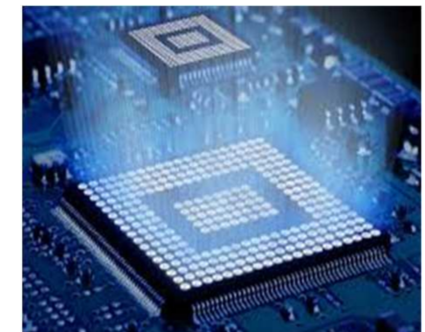


How these technologies can boost

Image sensor



HPC

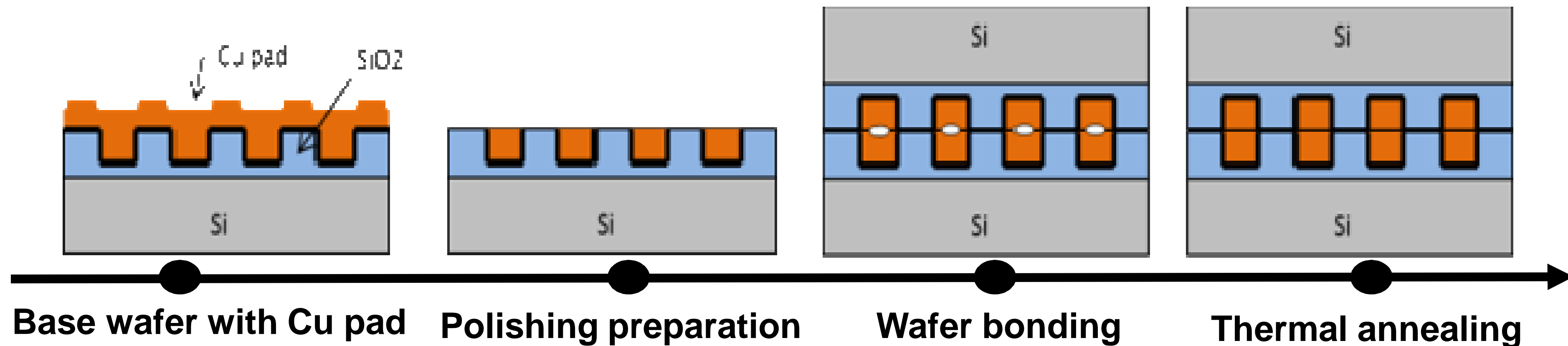


OVERVIEW

1. 3D VLSI technologies: from hybrid bonding to 3D sequential integration
2. 3D imagers
3. High Performance computing

3D VLSI: HYBRID BONDING AND 3D SEQUENTIAL OPTIONS

Hybrid bonding flow:



Various options: Wafer to Wafer, Die to Wafer, Die to Die

3D VLSI: 3D SEQUENTIAL INTEGRATION

contact

3D contact

Bottom MOSFET process with or wo interconnects

Top active creation: Future MOSFET channel

Top MOSFET process

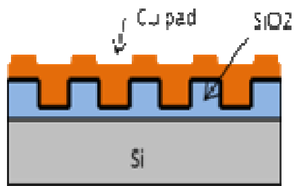
3D contact BEOL

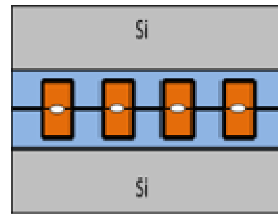
Also named 3D monolithic

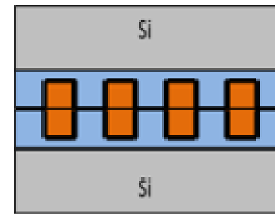
THERMAL BUDGET CONSTRAINTS

… CoolCube™

3D VLSI: HYBRID BONDING VERSUS 3D SEQUENTIAL

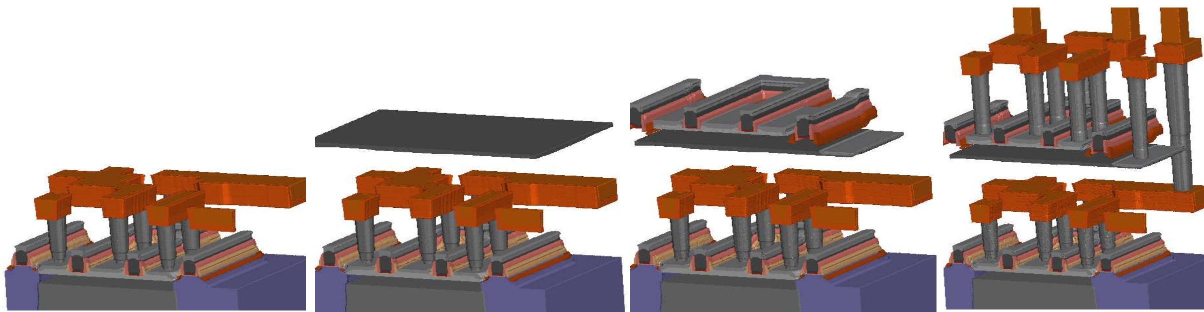






Hybrid bonding

Alignment made during bonding
3σ min = 250nm

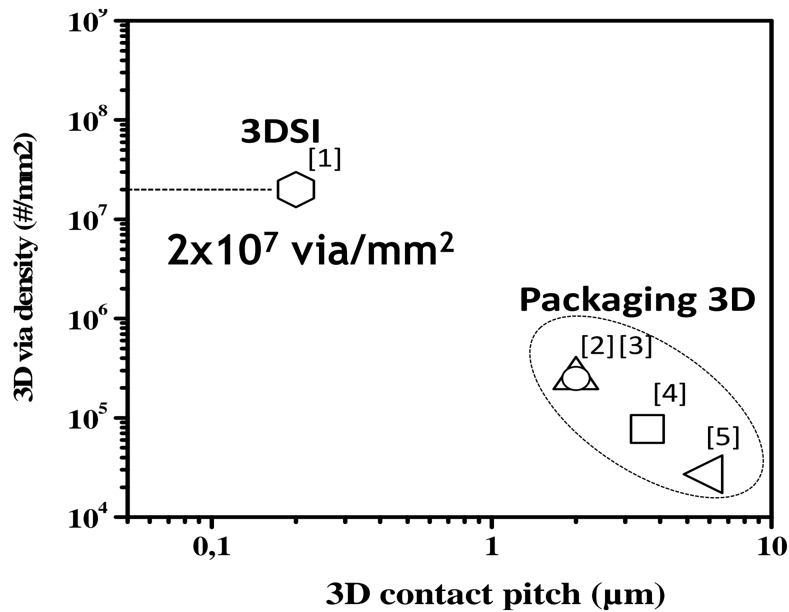


3D sequential

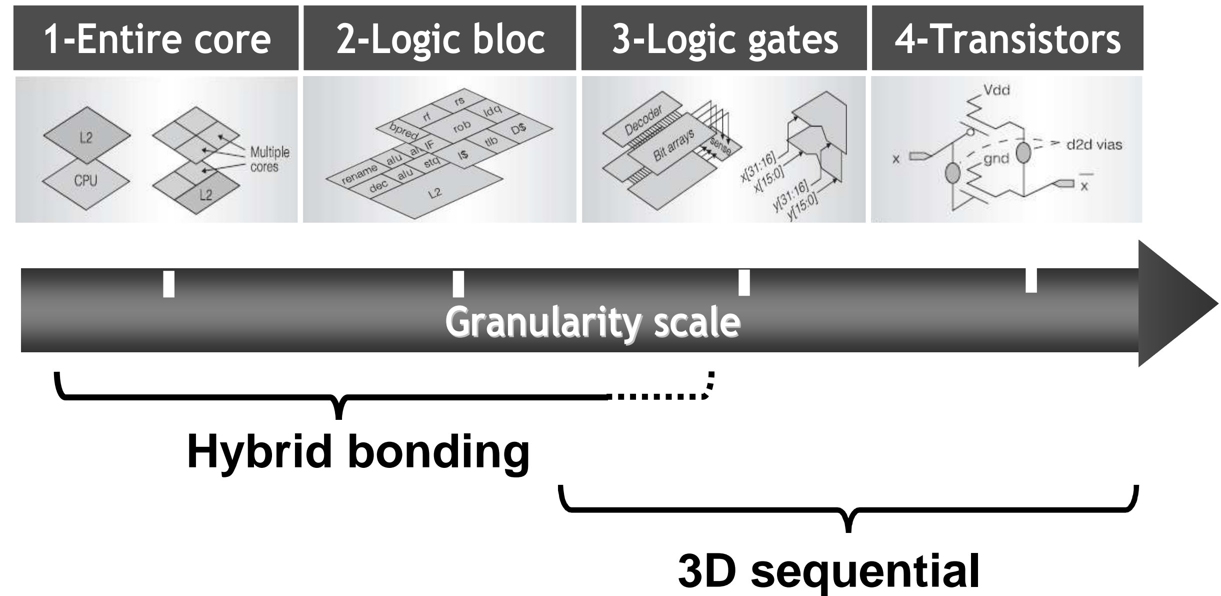
Alignment by lithography
3σ = 5nm (28nm stepper)

3D VLSI: HYBRID BONDING & 3D SEQUENTIAL OPTIONS: VIA DENSITY

3D via density



3D partitioning options



[1]: L. Brunet et al., VLSI 2016, [2] I. Sugaya et al., ASMC 2015, [3] J. De Vos, 3DIC 2016
[4] L. Peng et al., EPTC 2016 [5] D. Zhang et al. TSM 2015

OVERVIEW

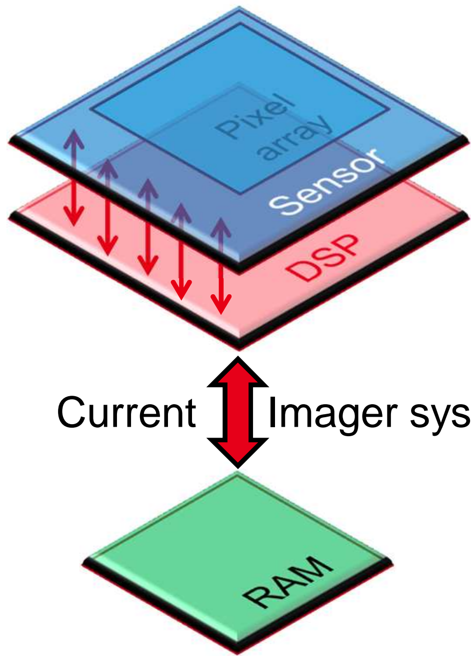
1 3D VLSI technologies: from hybrid bonding to 3D sequential integration

2 **3D imagers**

3 High Performance computing

3D IMAGERS: CURRENT PARTITIONING TRENDS

2-layer imager + DRAM

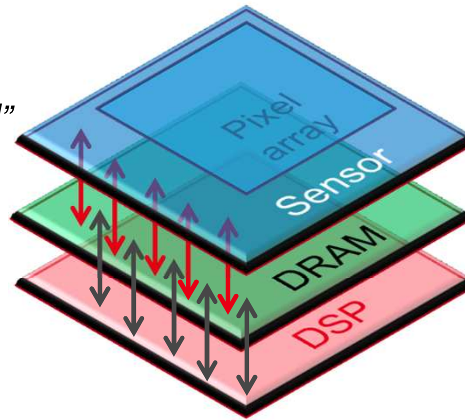


Current Imager system

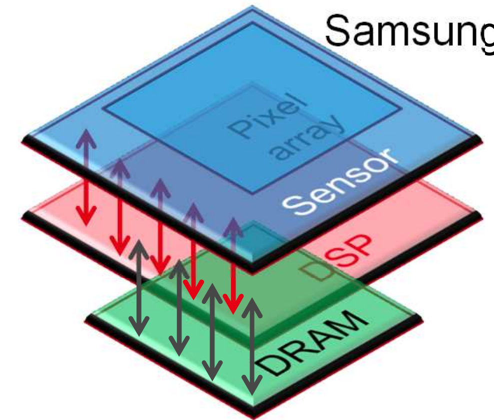
3-layer stack

Sony [2]

"Motion Eye™"

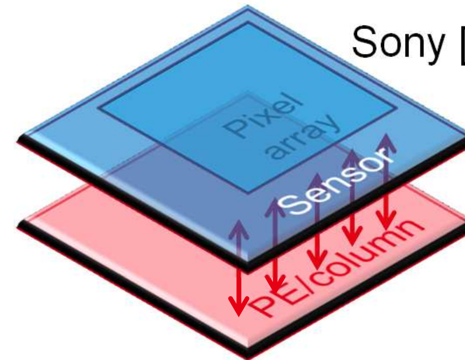


Samsung



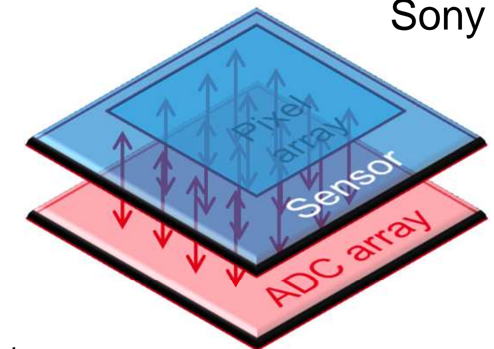
parallel processing

Sony [3]



Conversion and processing at column level
1 ADC + 1 PE / column

Sony [4]

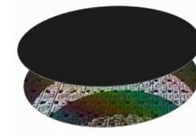


Parallel access to pixel array
1 ADC / 10x16 pixels

Form & Fill factor gain wrt 2D
Energy efficiency and performance[1]

[1] Retine leti [2] SONY ISSCC 2017 [3] SONY ISSCC 2017, [3] SONY VLSI 2017

HYBRID CU BONDING (WTW)



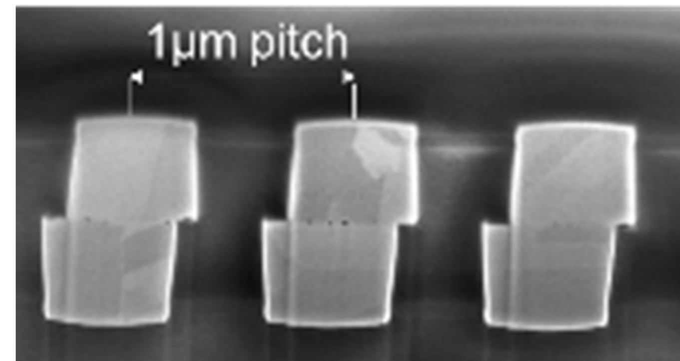
Alignment

Co-development equipment/process

Advanced bonding tool generation (Gemini)

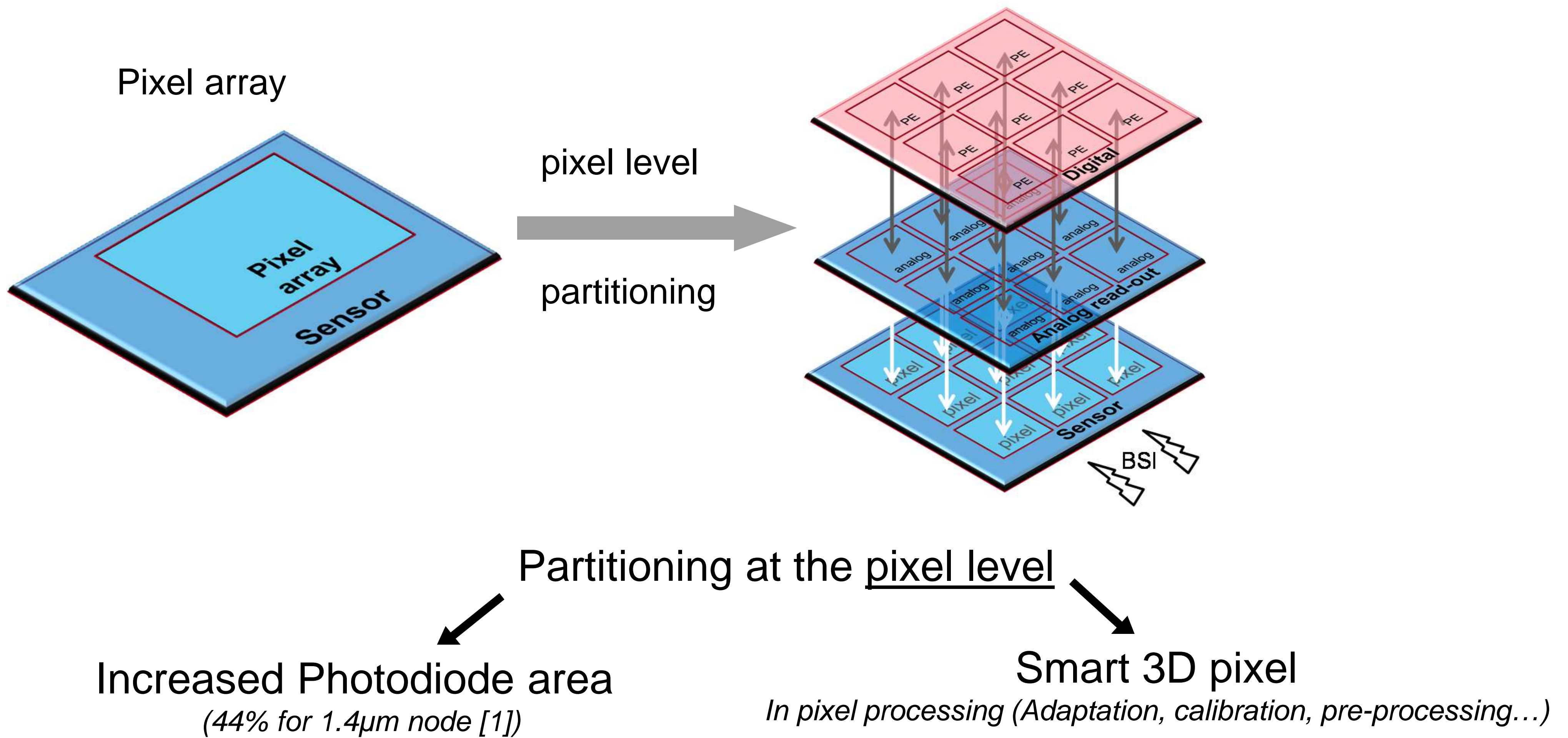
→ Alignement performance: 3σ = 195nm

1µm pitch Hybrid Bonding



[1] A. Jouve, S3S 2017

3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES



Partitioning at the pixel level

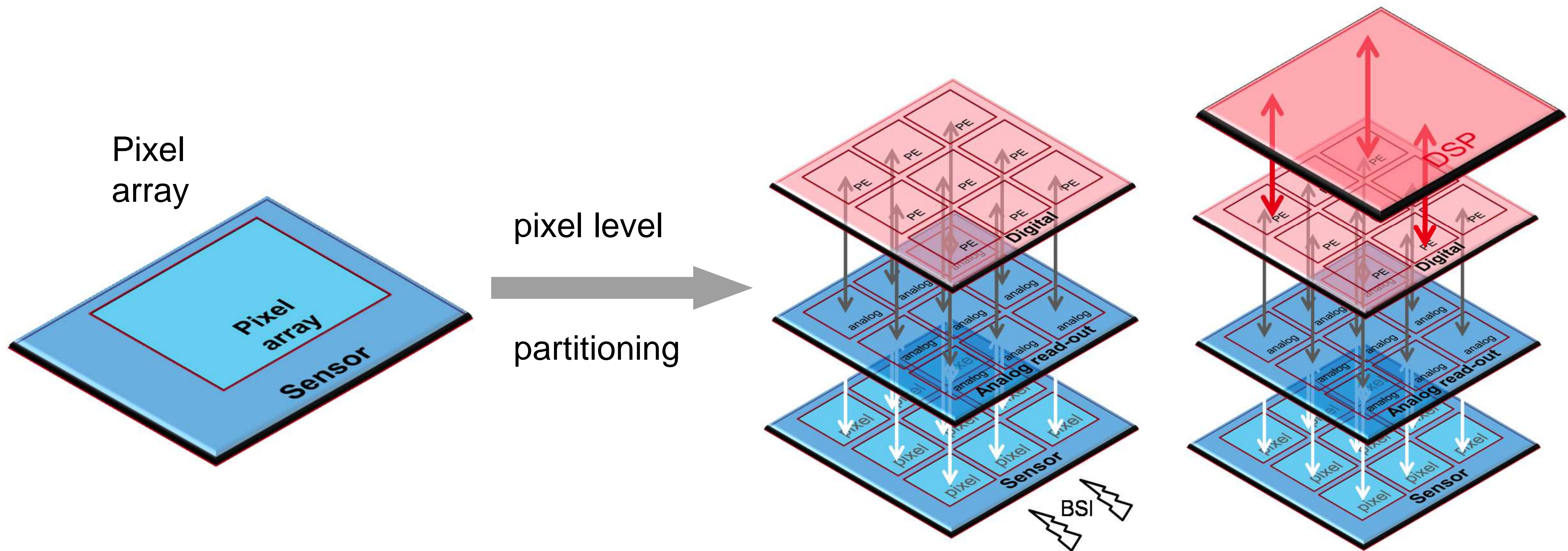
Increased Photodiode area

(44% for 1.4µm node [1])

Smart 3D pixel

In pixel processing (Adaptation, calibration, pre-processing…)

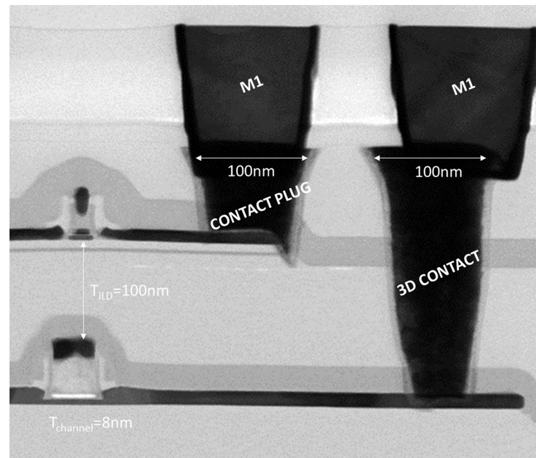
3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES

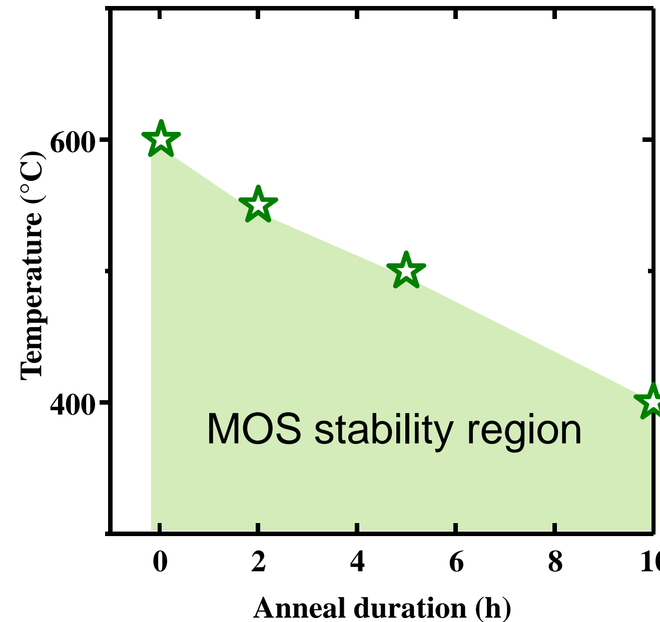


Hybrid bonding can be used to connect the 3D pixel to the DSP and RAM

3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES

<1µm 3D contact pitch ⟶ 3D sequential integration



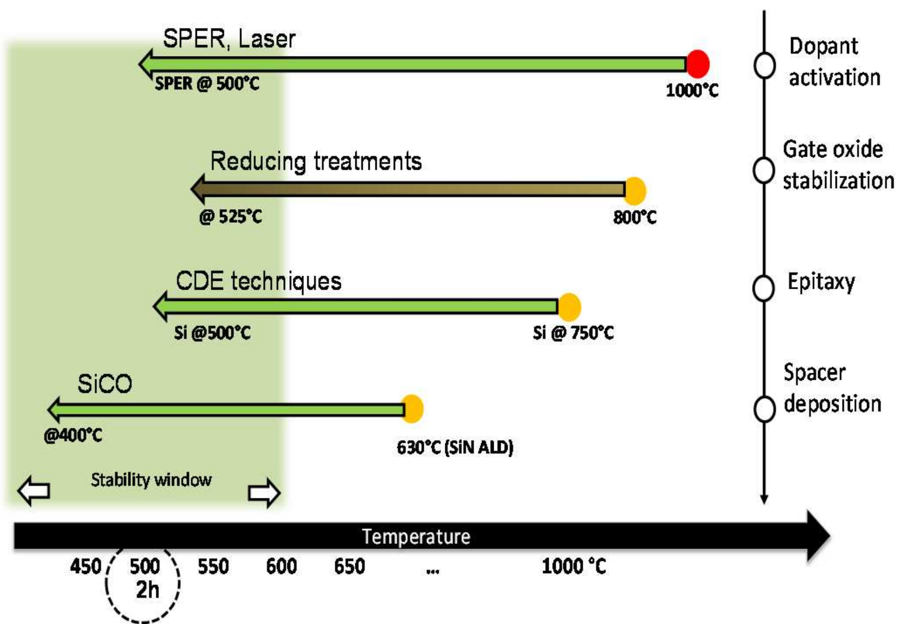


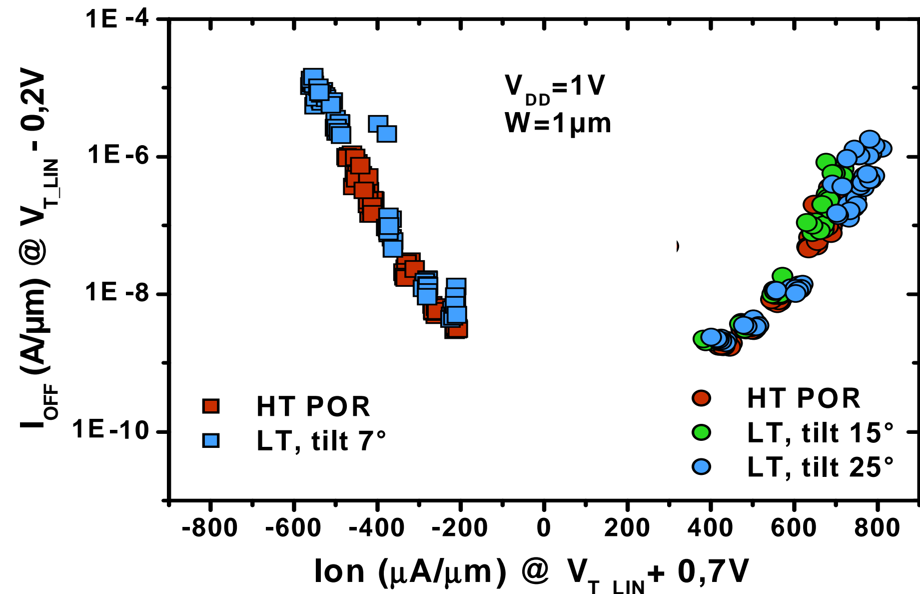
300 mm industrial clean room demonstration

Max TB budget is relaxed for a photodiode (700°C) [1] vs MOSFET (500°C)

[1]P. Coudrain et al., IEDM 2008

3D IMAGERS: NEW PARTITIONNING OPPORTUNITIES





Critical process modules are now below 500°C

Cold 28nm FDSOI devices in line with high-temp. POR

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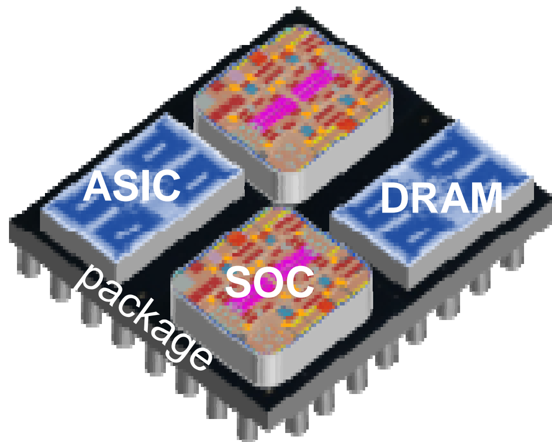
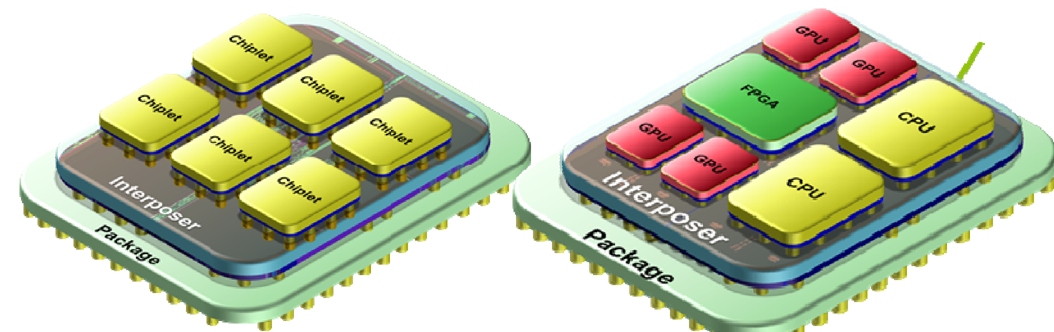
REVISITING HPC CHIPS ARCHITECTURE

Complex SOC for HPC application



Leti's roadmap: Chiplets on active interposer



Intact 3DNOC [1]
FDSOI 28nm on C65

Perspectives

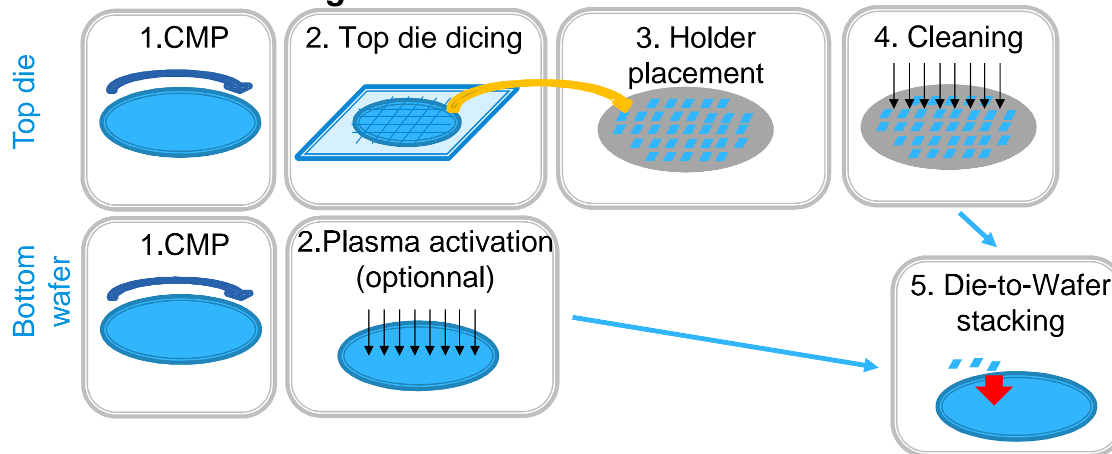
Huge die size (4cm²) (yield issues)
Complexity wall (co-integration of technologies)
Memory wall

Cost reduction:
Smaller chips (improved Yield)
Known good die (pre bond test)
Each technology at the right silicon cost

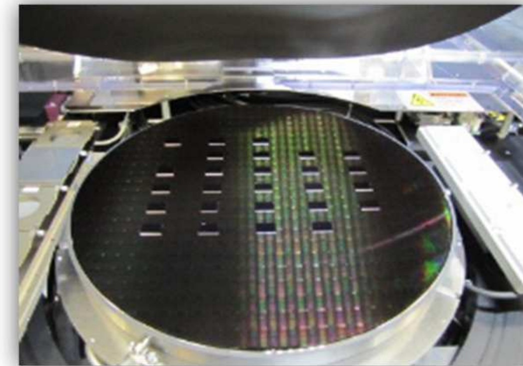
Performance:
Best technology for each chip
Compatible with HBM

[1]: P. Vivet et al., ISSCC 2016 (leti)

DIE TO WAFER WITH SCALED CONTACT PITCH



Smart Equipment Technology



FC1 Results

- Precision: ± 1 µm
- Throughput: 500 dph

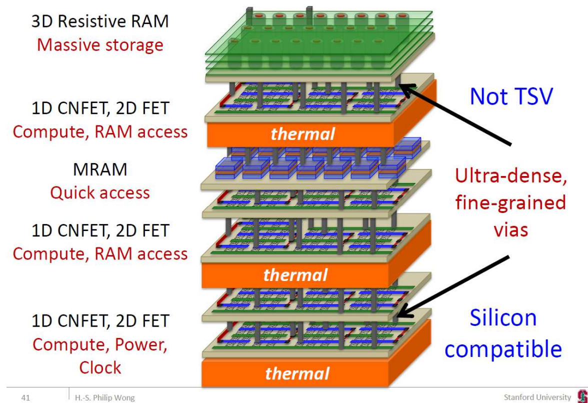
3µm pitch DTW hybrid bonding demonstrated

[1] P. Metzger & Al « Toward a flip-chip bonder dedicated to direct bonding for productionenvironment », IWLPC 2017.

THE ULTIME IMBRICATION OF MEMORY AND COMPUTING

→ 3D sequential is an opportunity to break the memory wall

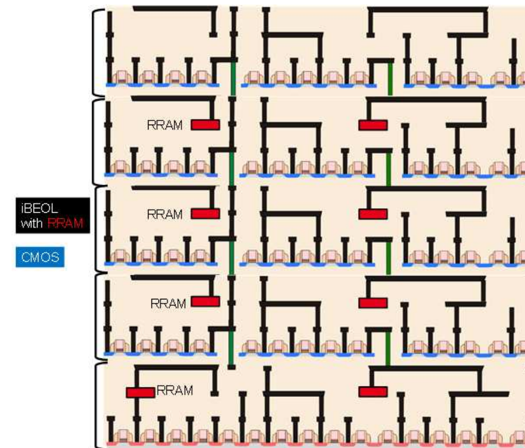
Computing immersed in memory



N3XT Computing system [1,2]

X 1000 gain in consumption expected with computing near memory

Neuromorphic computing



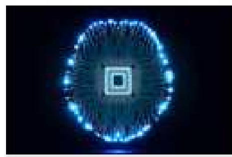
Brain-inspired computing cube

- High contact density mimics the high interconnectivity of neurons
- RRAM mimics the synapses

[1] Shulaker et al., IEDM 2014 , [2] Aly et al., Rebooting computing, 2015

CONCLUSION: LETI 3D OFFER

- Every application recquiring a high number of interconnections or reconfigurability of the interconnections deserves to be explored in 3D

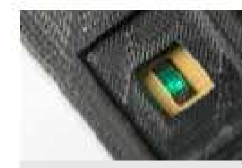

Neuromorphic Accelerators

Implants & Wearables

HPC

Imagers

Lighting


Displays

- Leti is your partner to evaluate the gains for your applications using 3DVLSI

- Demonstration of prototypes & Architecture partitionning

Thank you for your attention