

SILICON-BASED QUANTUM COMPUTING

TOWARDS EFFECTIVE, MANUFACTURABLE
QUANTUM COMPUTING



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CEA-LETI: BUILDING A SILICON-BASED PATH TO EFFECTIVE, MANUFACTURABLE QUANTUM COMPUTING

Since the 1940s, semiconductor technologies have enabled development of increasingly capable computers, with today's extraordinarily powerful systems utilizing fingernail-sized pieces of silicon that contain billions of transistors. Now, there is wide interest in extending these capabilities even further with a concept first theorized in the 1980s: the use of quantum phenomena to perform computation. Early experimental demonstrations suggest that the ability to harness quantum physics to solve extremely challenging problems may be coming within reach.

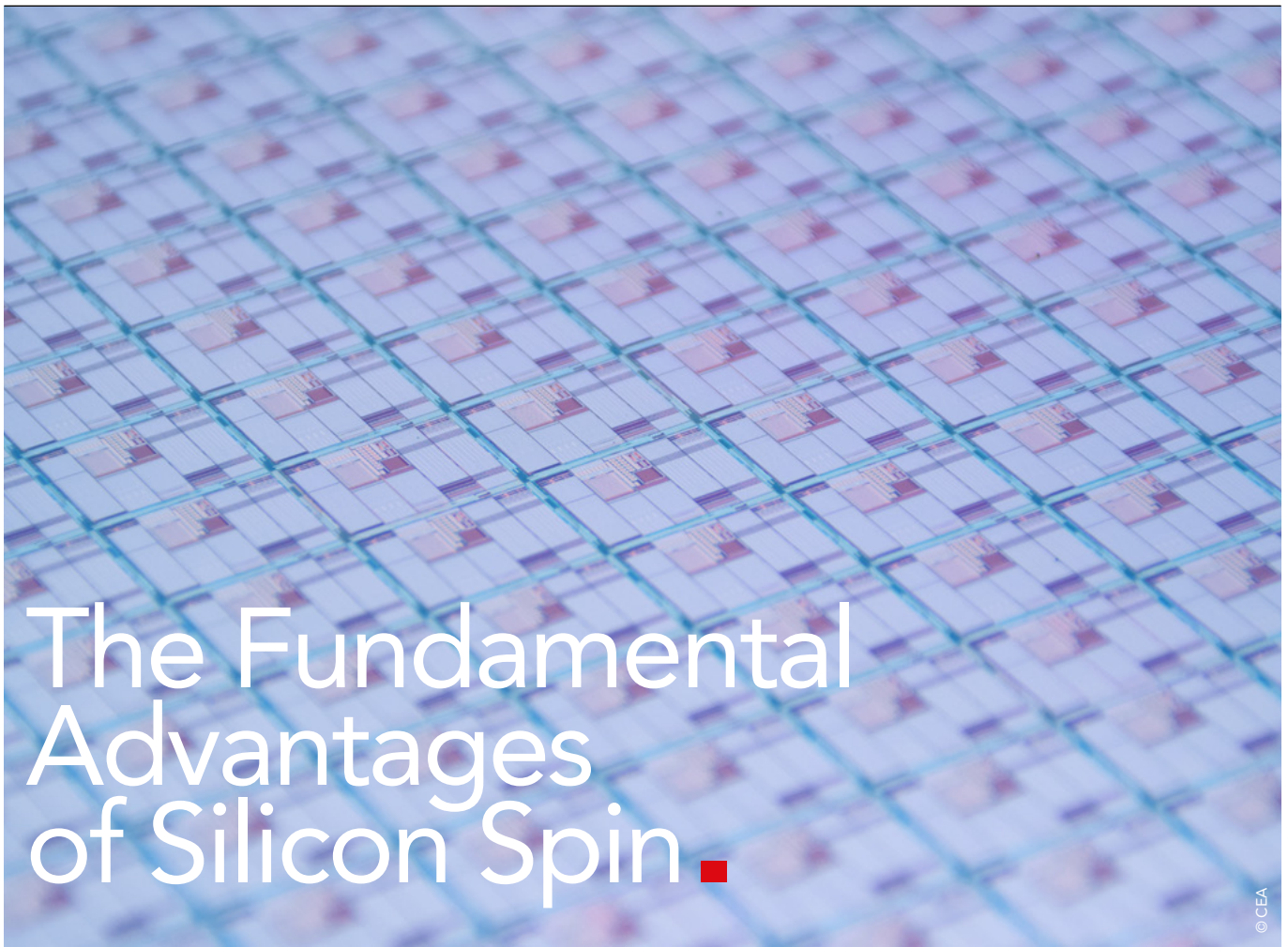
Diverse experimental platforms have been evaluated in the quest to fabricate qubits, the quantum bits that are broadly analogous to the bits used in classical computing. Many organizations around the world are pursuing these capabilities, along four primary paths:

- Superconductors
- Photonics
- Trapped ions
- Electron spin within semiconductors (silicon)

It's too early in the process to declare a "winner," and different approaches might prove to be suitable for different applications. But there is good reason to think that the silicon-based approach, in which semiconductor devices are used to create arrays of electrostatic-potential traps to isolate single electrons, is a leading candidate to meet three critical criteria:

- Effective on a fundamental level
- Manufacturable using well-proven processes and materials
- Able to be integrated with classical (silicon-based) computing systems

 ANNEX: CEA's long-standing quantum development efforts (p.19)

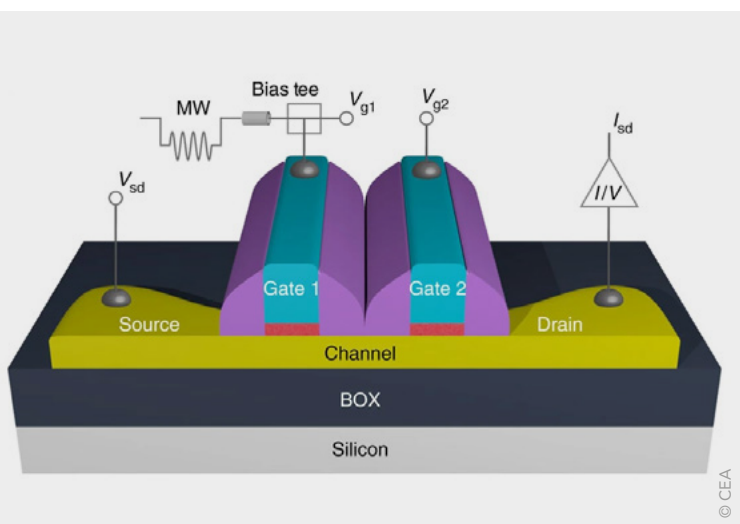


The Fundamental Advantages of Silicon Spin ■

The silicon approach, which leverages well-established CMOS technologies, still faces significant developmental challenges, but it offers a number of fundamental advantages that make it appealing as a way forward. Some of the most important of these are:

- Device operability at temperatures in the ~1K range, rather than the mK range (near absolute zero) required for superconducting approaches.** While this may not seem like a large difference, the difficulty of achieving and maintaining lower temperatures increases exponentially as they approach absolute zero. This extra margin in thermal budget allows for the operation of larger systems with more embedded classical control electronics.
- Improved resistance to decoherence, due to the characteristics of silicon.** The phenomenon of decoherence (see *ANNEX, CEA's Heritage of Quantum Research and the Silicon-Based Approach*) is a fundamental challenge to quantum computing, and one major source in semiconductor spin qubits is the interaction between the magnetic moments of electron
- and nuclei spins. While III-V semiconductor materials, as used in some photonic-oriented quantum development efforts, have non-zero total nuclear spins, the majority isotope of Si, ^{28}Si (which represents 95% of natural Si), has no net nuclear spin. Additionally, natural Si may be isotopically purified almost as far as needed (the state-of-the-art is above 99.99%) using centrifugation. It results in a remarkably clean magnetic environment for the qubits and therefore longer electron spin lifetimes.
- Speed of operation.** Thanks to a gate-defined structure that allows tight coupling, speed is in the μs range for all types of operations. This ensures reasonable calculation times, on the order of billions of operations per hour, which is well in line with the current state of the art in quantum processing.

- The ability to isolate single electrons within a structure fabricated using CMOS technology.** This provides enhanced control over the qubit. As CEA-Leti researcher Maud Vinet put it in a recent interview, the structure is, in essence, "a transistor with huge access resistance. [In that configuration], it's going to be very easy to [create] a potential well between your two resistances, a quantum dot. And then in this potential well, you can actually trap an electron and come and manipulate its spin with a magnetic field. And this is the story of silicon-spin qubits." To fabricate the quantum dots, CEA-Leti leveraged its FD-SOI platform because it offers several advantages. First, it allows application of capabilities from CEA-Leti's FD-SOI cryo-CMOS efforts, which have developed CMOS technologies that can operate at cryogenic temperatures. Also, in the development phase, it enables the use of a "back-gate" below the devices to provide in-situ control of the potential wells, which confine the qubits. And additionally, in the context of fabricating a full-stack quantum processor unit with integrated low-temperature control electronics, FD-SOI appears to be a technology of choice — use of the same technological platforms for qubits and control electronics simplifies co-integration.
- High integration density, which facilitates scalability to larger arrays of qubits.** The semiconductor industry has the unique capability to easily and economically fabricate billions of identical micro-structures, such as transistors. Early work done at Quantum Silicon Grenoble has demonstrated the ability to fabricate multi-layer structures that place CMOS quantum dots in close proximity to single-electron transistors (SETs) with typical spacings of 100nm. This would allow up to 106 qubits to be built in a 100-micron-square (0.1mm) area, with the opportunity for parallel operations — important considerations for a large-scale quantum computing architecture.



WORLD'S FIRST QUBIT DEVICE FABRICATED IN STANDARD CMOS PROCESS

Simplified 3D schematic of a silicon-on-insulator
nanowire field-effect transistor with two gates

THE OVERARCHING VIRTUES OF MANUFACTURABILITY & INTEGRATION

Beyond the quantum-level considerations described above looms a broader issue: quantum processors will have very limited utility and application if they cannot successfully integrate large numbers of qubits and conveniently interface with classical computers.

Note that, while quantum physics is a complex and challenging subject, much of the terminology used in the above discussion of silicon-based quantum technology will be familiar to anyone with experience in the semiconductor sector. The basic material, silicon, and CMOS technology have been the subject of intensive R&D and engineering work for well over half a century, and newer innovations like quantum dots, SETs, and FD-SOI materials are also quite well-characterized in comparison to technologies used in other approaches to quantum computing.

This provides rich reservoirs of basic scientific knowledge and implementation know-how that can be drawn on by researchers developing silicon-based quantum technology. It also means that existing equipment and processing techniques can be leveraged, which simplifies research, development, and the all-important transition to manufacturing that will be critical to the success of any approach to quantum computing.



CEA-LETI'S PRE-INDUSTRIAL FACILITIES

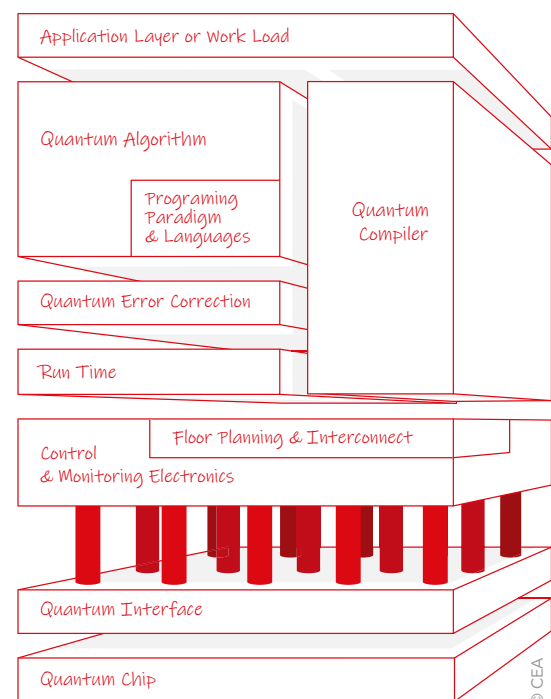
Grand Objective: Develop a "Full Stack" of Production-Ready Technology.

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A COMMITMENT OF NECESSARY RESOURCES AND EXPERTISE

One of the grand challenges of quantum computing development is the effective linking of groundbreaking laboratory research and proof-of-concept realization with prototyping, pre-industrialization activities, and subsequent productization and production.

Academic research organizations typically focus on the earlier stages, and private-sector companies on the later ones, but since its founding in 1967, CEA-Leti has followed a unique approach to developing "full stacks" of effective, manufacturable technologies that reach market successfully. This involves cultivating a combination of world-class facilities and personnel, fostering a working environment that takes a long view of the research-to-market process, and building strong relationships with companies (including established leaders, spinouts, and startups) and establishing scientific collaborations with leading research organizations and universities worldwide.



SOCLE COMPLET CEA-LETI

CEA-LETI'S QUANTUM ECOSYSTEM

The multidisciplinary expertise needed for quantum computing development transcends the capabilities of any single organization, even one with as much diversity as CEA. An especially wide range of disciplines is involved, from mathematics and physics to computer science, cryogenics, materials science, software development, and of course the many skills needed for advanced semiconductor design and production.

CEA-Leti has longstanding pre-existing partnerships in many of these areas, with organizations like the Néel Institute at the French National Centre for Scientific Research (CNRS), CEA-List, CEA-Irig, and CEA-Iramis, universities like MIT, Stanford, Cambridge, Université Grenoble Alpes, and the University of New South Wales in Australia, as well as dozens of leading technology-based corporations.

In 2018, CEA-Leti, Institute Louis Néel from CNRS, University of Grenoble Alps, and CEA-IRIG joined forces and formed the Quantum Silicon Grenoble group to work on silicon-based quantum computing. The group was awarded an ERC Synergy grant. The team's early accomplishments include publication of its breakthrough 28nm FD-SOI Quantum Integrated Circuit project at the ISSCC 2020 conference and expansion of its operations in quantum engineering; it is continuing to pursue its goal of developing a scalable quantum processor based on state-of-the-art silicon technology.



▶▶ A new chapter is being opened by CEA-Leti's selection as coordinator of the EU's four-year Quantum Large-Scale Integration with Silicon (QLSI) consortium ([read press release on CEA-Leti website](#)).

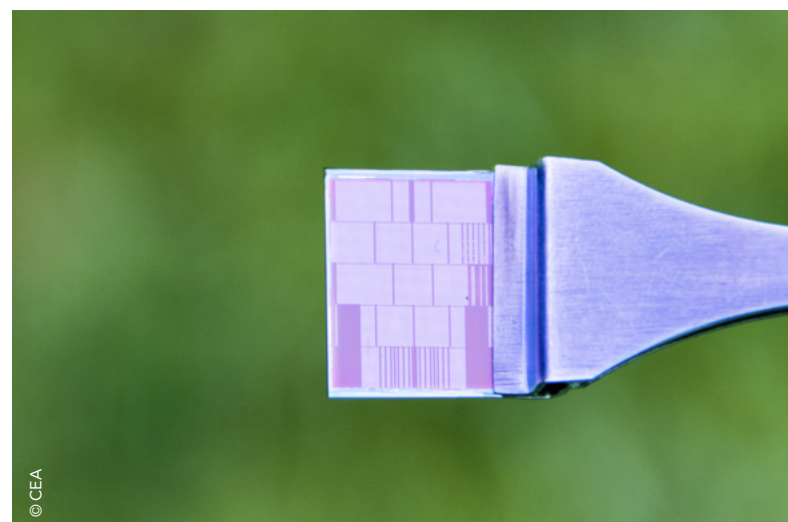
▶▶ ANNEX: Read more on CEA's Long-Standing Development of Silicon Resources (p. 20)

YOUNG TALENTS

In 2016, CEA-Leti joined the local multidisciplinary QuEnG network (Quantum Engineering Grenoble). Building on the unique concentration of expertises in Grenoble, QuEng is training outstanding students to become the future quantum engineers.

CEA-LETI COORDINATING EUROPEAN PROJECT TO SCALE VERY LARGE NUMBERS OF SPIN QUBITS

As coordinator of the pan-European QLSI Project, CEA-Leti is leading the pursuit of industrial-scale implementation of semiconductor quantum processors with a focus on demonstrating that silicon-spin qubits are the leading platform for scaling to very large numbers of qubits.



ADDRESSING THE CHALLENGES OF SEMICONDUCTOR SPIN QUBITS

To implement its solid silicon-based technology expertise in the quantum sphere, CEA-Leti has, as of January 2021, a diversely skilled team of more than 50 people working on quantum development, with a large portion holding doctorates and post-doctoral qualifications. Expertise includes micro- and nanoelectronics; simulation and modeling; 2D and 3D materials; device architecture and design (including both logic and memory); mask development; 3D integration and packaging; integrated circuits; physical characterization (in-line and off-line); electrical characterization and reliability; the emerging field of ultralow temperature cryo-CMOS; and software. These skills are complemented by CEA-IRIG and CNRS who are experts in quantum engineering, physics of scaled nanostructures, quantum physics.

CEA-Leti, CEA-IRIG, and CNRS share more than 7 cryogenics equipments as well as operation expenditures in the silicon platform and capital expenditure include the acquisition of a novel cryogenic wafer prober (from the leading cryogenic company Bluefors) for automatic measurements of 300mm wafers down to temperatures of 2K.



CEA-LETI BUYS A NEW CRYOGENIC PROBER TO CHARACTERIZE QUANTUM CHIPS AT VERY LOW TEMPERATURE

The institute's acquisition of an automatic cryogenic prober from the Finnish manufacturer Bluefors notably strengthens development infrastructure, with the ability to run massive electrical tests at a full 300mm wafer scale, from DC up to gigahertz frequencies, in a temperature range between 20K and 2K.

[!\[\]\(0ac73c45806a78de248a19d9a2dbe7a6_img.jpg\) Read press release on CEA-Leti website](#)

How does the CEA-Leti organization intend to apply these intellectual and physical resources to create qubits using silicon?

From a strategic perspective, it's important to keep in mind that, in principle, silicon-spin represents perhaps the simplest path towards implementation of a two-level quantum system.

A powerful example of this potential came with the ISSCC 2020 publication, which described the 28nm FD-SOI Quantum Integrated Circuit (QIC) developed by CEA-Leti, CNRS and CEA-Irig through Quantum Silicon Grenoble. The device represents the first demonstration of integrating conventional electronic devices and elements with quantum dots on a CMOS chip, combining crucial analog and digital instrumentation with quantum structures fabricated on the same semiconductor layer.

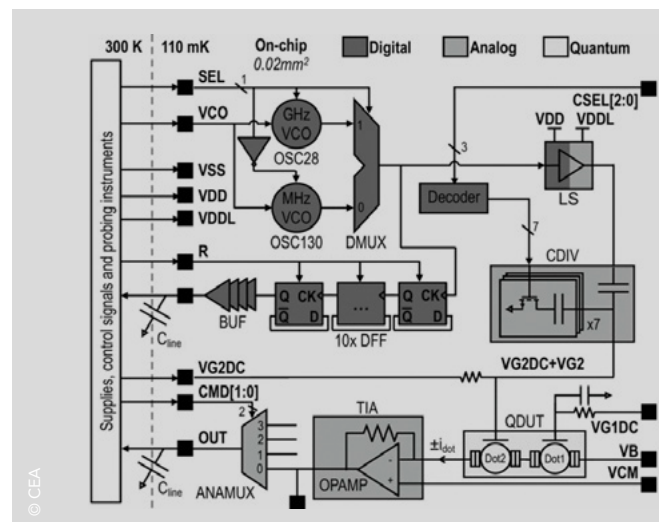
As the ISSCC paper stated, "the quantum silicon choice allows the IC community to integrate large-scale qubit-control electronics directly [adjacent to] the quantum silicon core, thus drastically reducing the wire-connection number and qubit-addressing fanout, meanwhile increasing the operation bandwidth for error correction and the spin-readout sensitivity."



Loïck Le Guevel, a lead author on the paper and member of the Quantum Silicon Grenoble research group led by Maud Vinet, noted that the device "uses all elements required to properly design high-spec state-of-the-art circuits, such as passive elements, resistors and capacitors, transistors for digital operation up to 7Ghz, and transistors for analog operation up to 3Ghz. On top of that, we were able to design a double quantum dot in the same semiconductor layer as transistors using a standard fabrication flow. This realization emphasizes that FD-SOI could one day allow circuit designers to use qubit arrays embedded in IP blocks with classic electronics to build custom-made, large-scale quantum silicon processors."

QUANTUM CIRCUIT

Functional block diagram of the mixed digital-analog signal circuitry interfacing a quantum device at 110mk



LOOKING MORE DEEPLY INTO THE REMAINING CHALLENGES



But on a more granular level, how are these capabilities achieved, and what challenges remain?

Let's detail what is needed to create a quantum computer:

First, quantum dots need to be defined and filled with one electron. Electrostatic gates, similar to those in classical transistors, can be used to define quantum dots. At cryogenic temperature, the individual electrons (or electron holes) held in them can be controlled using the tunnel effect. Application of an external constant magnetic field creates the two-level system.

Then, single and two-qubit operations need to be performed. Single-qubit manipulation is then obtained, for example, by applying a small microwave magnetic field. Each of the numerous qubits experiencing this microwave magnetic field can be made sensitive or insensitive thanks to a local applied electric field that changes the qubit resonance frequency (Stark effect). Two-qubit operations are realized by varying the interaction between two adjacent quantum dots. To switch the interaction on and off, researchers can detune the gates used for the quantum dots or add an additional interaction gate (or exchange gate) between the two dots.

Finally, the state of the qubit needs to be measured, in the so-called readout operation. Readout results from a spin qubit come from a spin-to-charge conversion, which is obtained by coupling the qubit with an additional quantum dot or single-electron transistor (SET). The spin of the qubit can be probed by detection of the change of charge or capacitance.



From a technology perspective, there is still an open question for large scale quantum computer: what is the optimal distance between quantum dots?

The spacing between the silicon-spin qubits produced in CEA-Leti laboratories is typically 100nm. These dimensions can be reached thanks to immersion lithography.

After some 70 years of work on transistor scaling in pursuit of Moore's Law advances in processing power, we have extensive ability to produce millions of identical objects with high yield and low variability. This is seen as a key asset in the effort to define, operate and read qubits in a reliable and repeatable manner.

However, even this is not enough to make quantum computing a reality. Leveraging this remarkable opportunity will require several other critical challenges to be addressed: Qbit Wiring, Cryogenic Electronics, Cryogenic Integration, System-Level Low-Temperature Design.

Qubit Wiring

To perform universal computation with qubits, it's necessary to have individual control of each and every qubit within an array of qubits. Such arrays of qubits are conceptually analogous to arrays of pixels, like those in CCD sensors or memory arrays. Thus, any practical quantum computing model could take advantage of existing know-how for addressing pixels within an array to control qubits on a large scale.

The ERC project team has developed a complete architecture that leverages 3D sequential integration and takes into consideration all the technological and physical constraints, and uses two layers of silicon to perform all the quantum operations. Known as Qucube, it is structured to implement a scalable spin qubit architecture in silicon and to perform large-scale quantum operations with electron spin qubits.

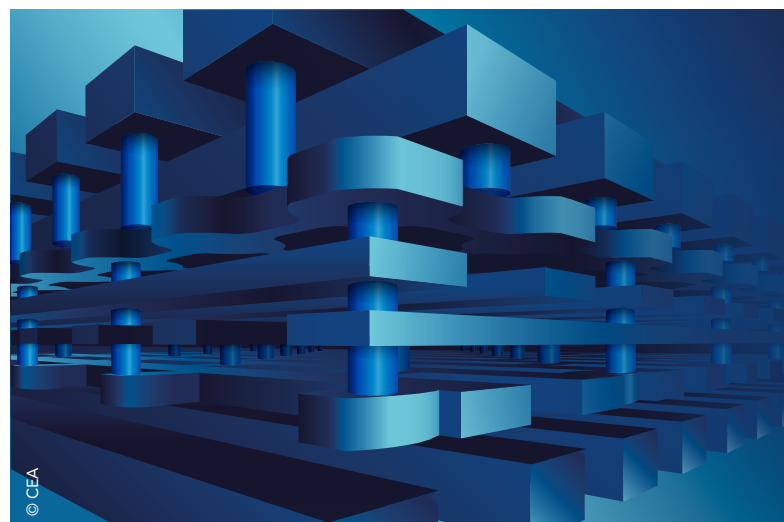
Another QSG effort recently published results aimed at improving quantum dot control and addressability, through the use of embedded detectors and an array of eight MOS quantum dots. The researchers evaluated two methods, a single-lead charge detector and a reprogrammable single-electron transistor. They found great promise for the ability to build a device with a large number of quantum dots, with the two methods offering the ability to perform real-time measurement of a single charge-tunneling event, which could be used to load single electrons in the structure or read out spin states.

It's also necessary to find ways to perform basic operations in parallel. The whole point of applying many more qubits to a task is to increase algorithmic efficiency; it's imperative that the scale-up to hundreds or thousands of qubits does not increase the execution time. One promising line of work by a CEA-Leti group is pursuing the ability to read out a full line of qubits in parallel using RF.

While substantial development is still needed, CEA-Leti's fundamental approach offers a very promising path to successful qubit interconnection.

3D ARCHITECTURE, CRYOGENIC LARGE SCALE COMPATIBLE ARCHITECTURE

Spin qubit architecture in Si to perform large scale quantum operations with electron spin qubits.



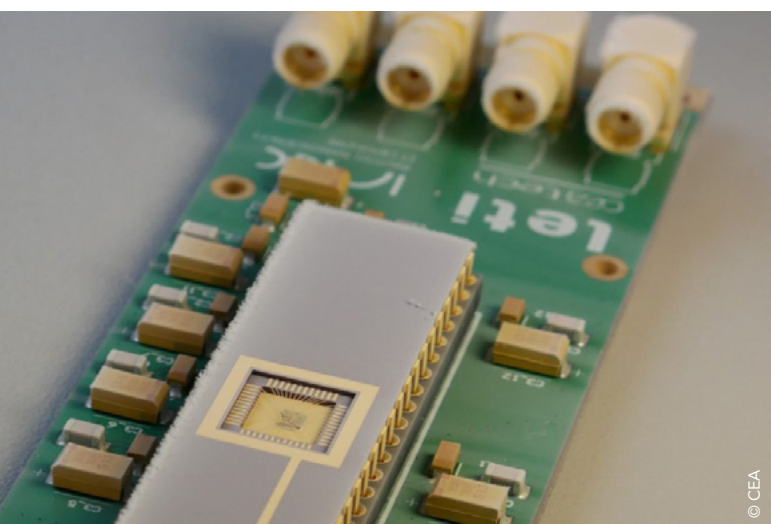
Cryogenic Electronics

Many of the basic challenges of quantum computing are intertwined. The need for operation at cryogenic temperatures, for example, affects all approaches to quantum technology, not just silicon spin, and all approaches will also require electronics for qubit control and read-out, and interfacing with classical computing systems. This highlights the broad importance of exploring and developing low-temperature CMOS technologies, especially advanced technologies such as FD-SOI, which has the unique property of being able to change its threshold voltage (V_{th}) and recenter it as a function of the temperature.

In this context, it's worth noting that one advantage of silicon qubits is that they are robust enough to operate at higher temperatures than superconducting qubits. Experiments have shown that 1K is a reasonable target for silicon-spin operations, with promising early results on fidelity and coherence time — critical factors in creating reliable and robust computing systems. Operation in the 1K range, rather than the mK range (closer to absolute zero), would simplify many of the practical challenges of system operation as it enables larger power to be dissipated.

In addition, developers will need to find ways of effectively linking room-temperature instruments and systems with low-temperature systems without creating information bottlenecks on the inputs and outputs. While work on this is still in progress, it seems likely that it will not be possible to address each qubit "in the refrigerator" from a room temperature controller and that it will be necessary to develop router-type schemes of directing and multiplexing data. Again, the analogy with memory or CCD arrays is applicable; this is the source of the crossbar-addressing solution. While it reduces the need for wiring, it also requires extremely precise electrostatic control capabilities ideally located as close as possible to the qubit die.

▶▶ These types of needs are the driver of CEA-Leti's development of cryo-CMOS system-on-chip solutions using FD-SOI technology, which aim to make them the best solution for low-temperature electronics. This could provide an essential building block for any large-scale quantum processors, by enabling the design of scalable close-to-qubit cryogenic electronics for massive qubit matrix indexation and, ultimately, development of fault-tolerant universal gate-based quantum computers (details in p.15).



CEA DEMONSTRATES QUANTUM INTEGRATED CIRCUIT COMBINING QUANTUM DOT WITH DIGITAL-ANALOG CIRCUITS ON CMOS CHIP

This FD-SOI device integrates crucial analog and digital functions (multiplexer, buffer, signal amplifier, oscillator, level converter) that can fulfill future quantum instrumentation needs, along with quantum dot structures fabricated on the same semiconductor layer.

▶▶ [Read press release on CEA-Leti website](#)

FD-SOI AND QUANTUM

CEA-Leti's world-leading experience with SOI development has helped set the stage for its demonstration that fully depleted silicon-on-insulator (FD-SOI) technology is a good option for cryogenic CMOS applications.

The operation of circuits at cryogenic temperatures (<100K) is necessary in a wide range of applications such as infrared sensors, spatial applications, and cryobiology. More recently, CEA-Leti's researchers have been investigating their use in quantum computing, for reading and controlling quantum bits.

CEA-Leti has published findings on the performance and variability of 28nm CMOS FD-SOI technology for cryogenic applications, down to 100mK. This has provided some of the first experimental measurements and analysis of these circuits at cryogenic temperatures, including study of the drain current and transconductance of FD-SOI transistors, matching, self-heating, and low-frequency noise at temperatures <20K.

Cryogenic Integration

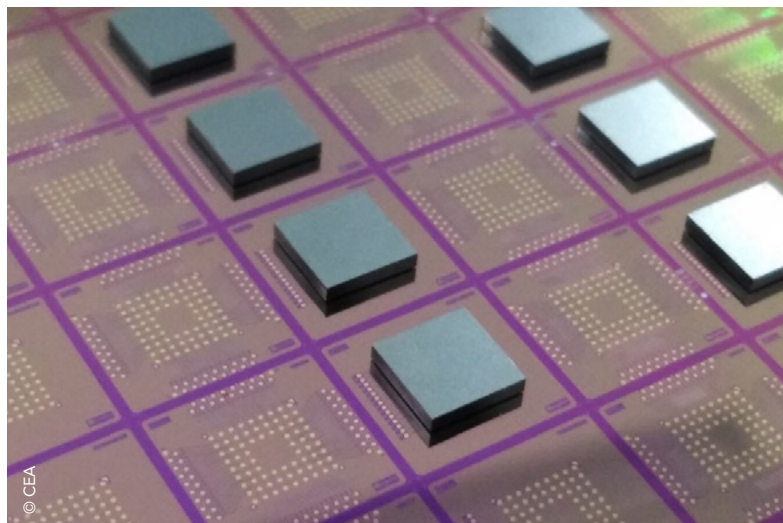
While the advances in basic cryo-CMOS capabilities are exciting, their successful application in practical systems will also require new capabilities in cryogenic packaging. To this end, CEA-Leti is leveraging its state-of-the-art 3D packaging line to develop novel silicon interposers that can be used to assemble quantum dies and their accompanying electronic controllers. The program opens a number of architectural options in terms of die size for qubits and cryo-CMOS, along with the possibility of integrating additional functionalities for transmission between qubits and cores.

The interposer project, which involves a team from CEA-Leti, CEA-List, CEA-IRIG, and the Néel Institute at the French National Centre for Scientific Research (CNRS), illustrates how multiple technological building blocks can be applied to address the many challenges that arise in a project of this scope and complexity.

CEA-LETI PAVES THE WAY FOR MASSIVE INTEGRATION OF QUBITS, CRITICAL FOR ACHIEVING QUANTUM SUPREMACY

Interconnections between quantum and classical devices are critical. This award-winning paper at the 2020 Electronics System-Integration Technology Conference reviews successful initial validation of existing die-to-wafer 3D interconnect technologies for operation at sub-Kelvin temperatures.

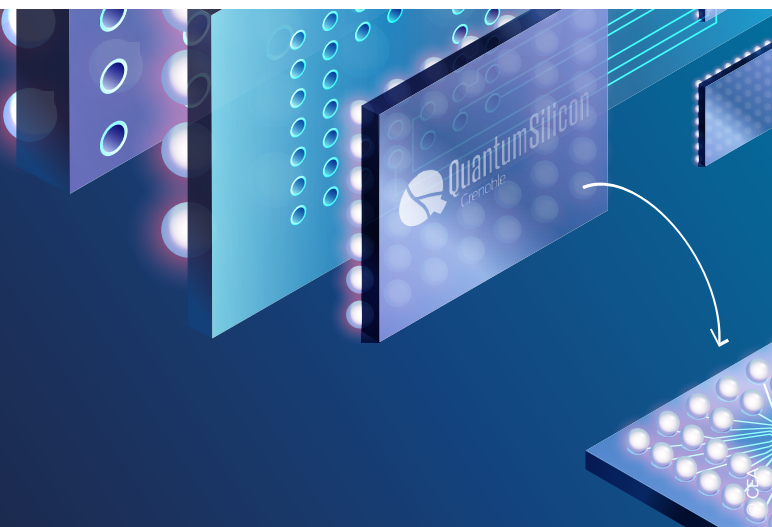
▶▶ [Read press release on CEA-Leti website](#)



The interposer's primary function is to accommodate and connect devices containing both quantum and classical elements, allowing the system to address and read qubits, while also enabling better technological control and easier co-existence of the two types of elements. This requires it to be conveniently compatible with both quantum and control components fabricated by different groups using different processes and materials.

One important advantage of the interposer design is that the qubits and control electronics are coupled by routing lines on the interposer, rather than with a wire-bonding approach. This reduces parasitic capacitance and inductance that complicate measurements. Moreover, through careful choice of materials and processing options, the researchers are working towards the challenging goal of having the interposer provide thermal decoupling of the quantum and control chips, so the quantum elements can be kept at the lowest possible temperature.

Subsequent efforts have focused on related advancements. One is the adaptation of existing CEA-Leti-developed flip-chip processes with die-to-wafer bonding techniques (such as SnAg microbumps and direct Cu-bonded pads with Cu/SiO₂ hybrid bonding) to fabricate interconnects that can operate reliably at temperatures below 1K. The CEA-Leti research team won a "best paper" award for their presentation on this achievement at the 2020 Electronics System-integration Technology Conference.



TOWARDS AN INTERPOSER PROTOTYPE FOR QUANTUM AND CONTROL CHIPS INTEGRATION AT VERY LOW TEMPERATURE

CEA-Leti's innovative approach for integration utilizes an interposer structure that embeds control electronics near the quantum chip inside a dilution cryostat at temperatures below 1K. CEA-Leti's successful realization of a demonstration 3D co-integration of quantum chips with cryo-CMOS FD-SOI 28nm control chips is an important milestone in the development process.



[Read press release on CEA-Leti website](#)

System-Level Low-Temperature Design

Finally, the overall system design for this type of novel low-temperature system will require careful and clever partitioning of different functions at different temperature stages.

For this reason, the CEA development teams include experienced analog and RF designers working closely with hardware architects and low-level-software engineers to develop a clear pathway to a fully operational integrated system. This will require system-level implementation of different elements (such as digital and analog hardware) at different temperature ranges

These efforts tie closely with the goals of the EU-funded QLSI project, particularly its targets of demonstrating a quantum computer prototype that integrates a high-quality quantum processor in a semi-industrial environment (with up to eight qubits available online), and documentation of the requirements for scalability towards large systems of over 1,000 qubits.

CEA-LETI TO BUILD QUANTUM-PHOTONICS PLATFORM TO ENSURE ULTRA-SECURE DATA FOR FINANCE, ENERGY, DEFENSE AND OTHER INDUSTRIES

Its extensive background in silicon photonics will be leveraged in this Carnot R&D project, which is focused on development of quantum-based ultra-secure data transmission capabilities. The three-year project will realize integrated qubit transmitters and receivers, and place them on a single platform for quantum computing applications.

▶▶ [Read press release on CEA-Leti website](#)



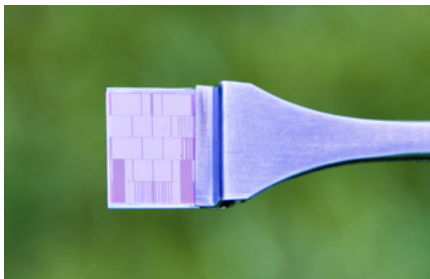
Conclusion

There are, to be sure, many remaining challenges in development of silicon-spin quantum computing. But the rapid and broad-based progress to date, and CEA's strong foundation of existing knowledge and development capability, are clear indications that its multi-institute, silicon-oriented approach to quantum computing has much to recommend it.

Expertise from an extraordinarily wide range of disciplines is needed, and the long heritage of CEA-Leti and the other CEA institutes in innovating, refining, and applying novel technologies is a perfect match for the demands of this exceptionally complex and challenging development process.

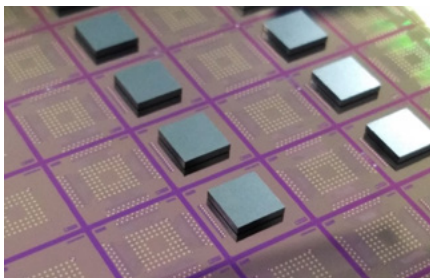


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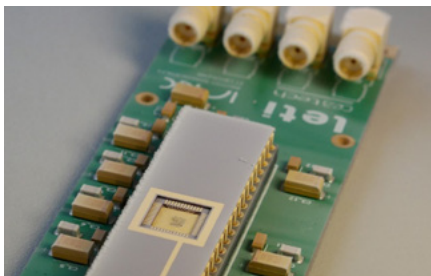
CEA-Leti Coordinating Project to Scale Very Large Numbers Of Spin Qubits, Position EU as Global Leader in Quantum Computing

As coordinator of the pan-European QLSI Project, CEA-Leti is leading the pursuit of industrial-scale implementation of semiconductor quantum processors with a focus on demonstrating that silicon-spin qubits are the leading platform for scaling to very large numbers of qubits.



CEA-Leti Team Paves the Way for Massive Integration Of Qubits, Critical for Achieving Quantum Supremacy

Interconnections between quantum and classical devices are critical to the development of quantum computing. This award-winning paper from the 2020 Electronics System-Integration Technology Conference (ESTC) reviews successful initial validation of existing die-to-wafer 3D interconnect technologies for operation at sub-Kelvin temperatures.



CEA-Leti and CEA-Irig Demonstrate Quantum Integrated Circuit Combining Quantum Dot with Digital-Analog Circuits on CMOS Chip

This proof-of-concept FD-SOI device integrates crucial analog and digital functions (multiplexer, buffer, signal amplifier, oscillator, level converter) that can fulfill future quantum instrumentation needs, along with quantum dot structures fabricated on the same semiconductor layer.



French Team on Route Towards an Interposer Prototype for Quantum and Control Chips Integration at Very Low Temperature

CEA-Leti's innovative approach to integration utilizes an interposer structure that embeds control electronics near the quantum chip inside a dilution cryostat at temperatures below 1K. CEA-Leti's successful realization of 3D co-integration of quantum chips with cryo-CMOS FD-SOI 28nm control chips is an important milestone in the development process.



CEA-Leti Buys a New Cryogenic Prober to Characterize Quantum Chips at Very Low Temperature

The institute's acquisition of an automatic cryogenic prober from the Finnish manufacturer Bluefors notably strengthens development infrastructure, with the ability to run massive electrical tests at a full 300mm wafer scale in a temperature range between 20K and 2K.



CEA-Leti to Build Quantum-Photonics Platform to Ensure Ultra-Secure Data for Finance, Energy, Defense and Other Industries

Its extensive background in silicon photonics will be leveraged in this Carnot R&D project, which is focused on development of quantum-based ultra-secure data transmission capabilities. The three-year project will realize integrated qubit transmitters and receivers, and place them on a single platform for quantum computing applications.

APPENDIX

CEA'S HERITAGE OF QUANTUM RESEARCH AND THE SILICON-BASED APPROACH

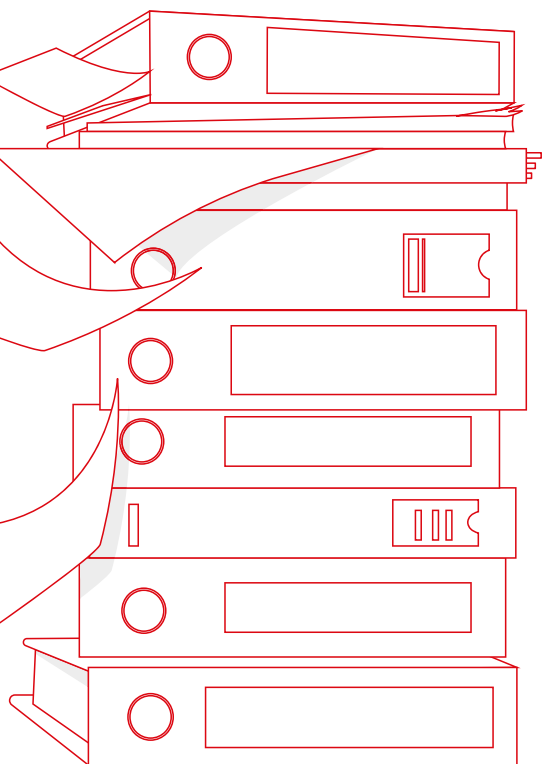
The idea that computers could harness quantum physics to solve problems on an unprecedented scale was born in the 1980s. Although quantum algorithms began to emerge, and researchers were able to create quantum systems in laboratories, the development of functional systems posed profound challenges.

Quantum computing systems typically seek to leverage the intrinsic angular momentum of electrons, or spin, as a means of representing data. But spin cannot be completely isolated from the external environment, and that makes it susceptible to decoherence — a quantum phenomenon that, in any quantum system, "transforms a coherent superposition of states into an incoherent mixture with random factors, and which causes the quantum bits to fall back to their minimum energy state," explains CEA-Iramis physicist Daniel Estève.

CEA, through its several centers of quantum physics research, has been involved in the field from its inception. Teams at the Iramis and Irig centers delved into electronic transport in quantum conductors (nanowires or contacts with a few atoms) and the quantum behavior of electrical circuits in general. They achieved a breakthrough with the 1998 development of a superconducting electrical circuit, the "Cooper pair box," which showed unprecedented decoupling from its environment and led to CEA's creation in 2002 of the first real, functional superconducting quantum bit, or qubit, with a hundred-fold improvement in protection against decoherence. In 2016, they demonstrated the first silicon spin qubit based on a CMOS industrial technology.

This line of superconductor-based work has been carried on at research facilities worldwide, including Yale University's 2007 development of the transmon superconducting charge qubit and CEA-Saclay's 2012 realization of an elementary processor with two transmons (i.e. four base states) and demonstration of an elementary quantum algorithm. However, there is some concern that superconducting approaches will not be scalable to the necessary levels of hundreds or thousands of qubits, due to the challenges of both decoherence and susceptibility to errors.

Based on this strong background, CEA's efforts have focused on leveraging standard silicon-based CMOS microelectronic capabilities in the service of quantum computing. "In 2016, we demonstrated that an elementary bit of quantum information can be encoded in the spin of a single electron, in excess or in default, located in an ultra-miniaturized CMOS transistor," explain CEA-Leti's Maud Vinet and CEA-Irig's Silvano De Franceschi, who received a European Research Council (ERC) grant in 2019 to continue their research.



APPENDIX

CEA'S LONG-STANDING DEVELOPMENT OF SILICON RESOURCES

Over the years, CEA-Leti has compiled an unmatched track record as it fulfills its mission to pioneer new micro- and nano-technologies. Relevant initiatives include:

- **Long-term development of silicon-on-insulator (SOI) technology,** a powerful enabler for semiconductors, microelectromechanical systems (MEMS), sensors, and now quantum devices. Work began in the 1980s, with the SmartCut® manufacturing process receiving a patent in 1991 and the successful startup Soitec launching the following year. Since then, the technology has been extended, including the development of fully depleted SOI (FD-SOI), and leveraged in partnerships with IBM, STMicroelectronics, and other leading tech companies, and in countless development projects.
- **Extensive work in fabricating a broad range of complex microstructures, including electronics, micro- and nano-electromechanical devices, sensors, and other functions.** CEA-Leti's pioneering work in wafer bonding, wafer-level packaging, 3D integration, materials development, and other related disciplines has paid dividends in hundreds of research projects and supported numerous startups.

Other CEA institutes are working on quantum computing, investigating other relevant paths.



APPENDIX

ADDITIONAL RESOURCES

- **EE Times Podcast Interview with Maud Vinet:**
<https://www.eetimes.com/podcasts/the-queen-of-quantum-•-space-docs-and-the-right-stuff-•-the-best-interviews/>
- **ACS Paper on Remote Capacitive Sensing in Two-Dimensional Quantum-Dot Arrays:** <https://pubs.acs.org/doi/10.1021/acs.nanolett.0c02393>
- **Princeton University Report on Silicon Spin Qubit Development:**
<https://www.princeton.edu/news/2019/12/30/leap-quantum-computing-silicon-quantum-bits-establish-long-distance-relationship>
- **ZDNet Report on University of New South Wales Advances in Silicon Spin-Orbit Qubit Coherence:** <https://www.zdnet.com/article/unsw-scientists-up-coherence-time-of-a-spin-orbit-quantum-computing-qubit-in-silicon/>
- **Nature Communication**, Maurand R, Jehl X, Kotekar-Patil D, Corna A, Bohuslavskyi H, Laviéville R, Hutin L, Barraud S, Vinet M, Sanquer M, De Franceschi S. "A CMOS silicon spin qubit" Nat Commun. 2016 Nov 24;7: <https://www.nature.com/articles/ncomms13575>
- **Solid State Electronics paper, "On the Modelling of Temperature Dependence of Subthreshold Swing in MOSFETs down to Cryogenic Temperature":** <https://www.sciencedirect.com/science/article/abs/pii/S0038110120300812#ab005>
- **ISSCC 2020**, Loïck Le Guevel et al., "19.2 A 110mK 295µW 28nm FD-SOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot" 2020 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA (2020): 306-308: <https://ieeexplore.ieee.org/document/9063090>
- **ICMTS 2020**, Bruna Cardozo Paz et al., "Integrated Variability Measurements of 28 nm FD-SOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications" 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), Edinburgh, United Kingdom (2020): 1-5: <https://ieeexplore.ieee.org/document/9107906>
- **IEEE Electron Device Letter**, Heorhii Bohuslavskyi et al., "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs Described With Band Broadening" in IEEE Electron Device Letters 40, no. 5 (2019): 784-787: <https://ieeexplore.ieee.org/document/8660508>

PROJECT ACKNOWLEDGMENTS

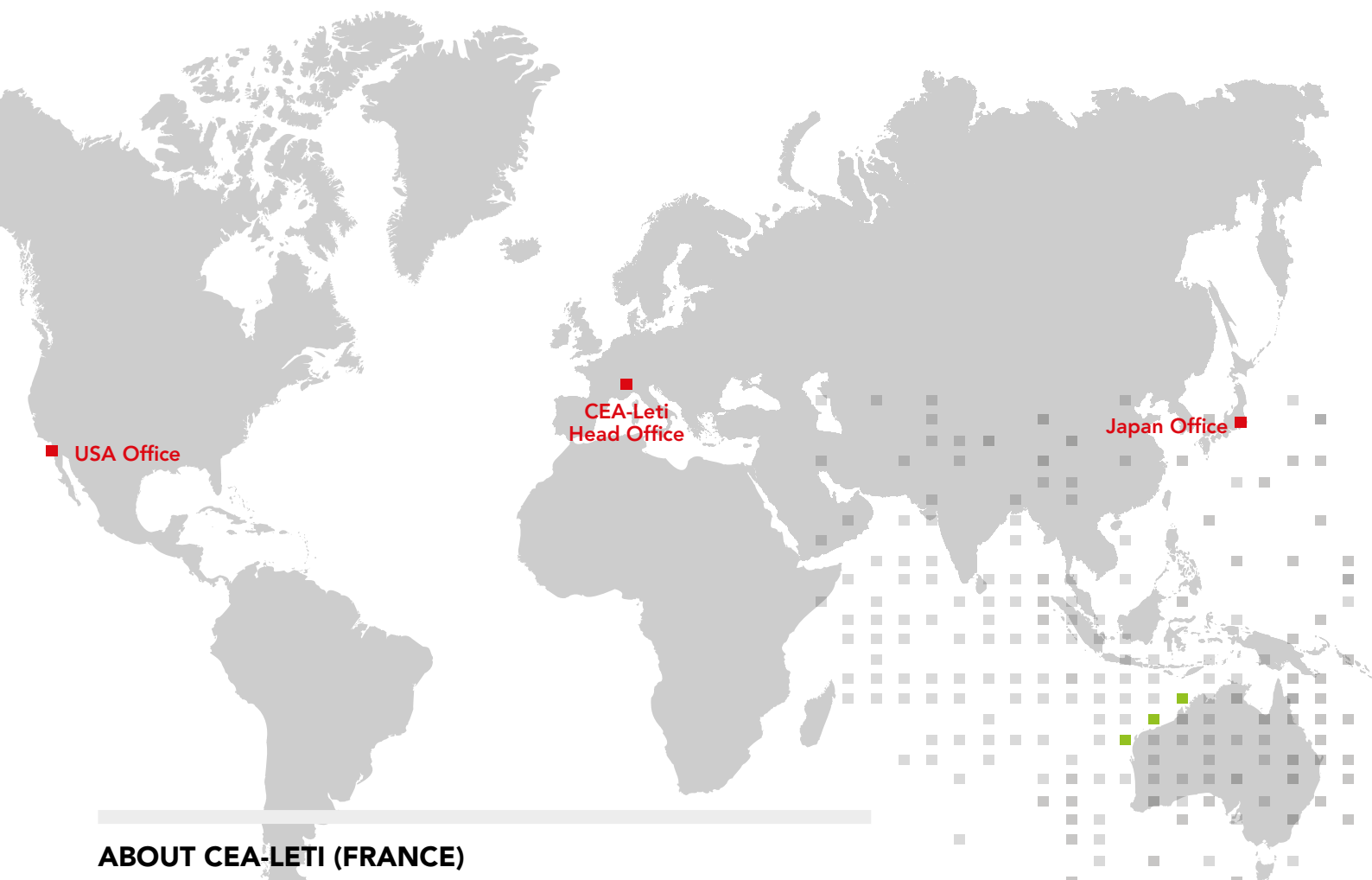
This work was partly supported by the European Union's Horizon 2020 research and innovation program under Grant Agreement No. 810504 (ERC Synergy project QuCube).

We acknowledge the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska-Curie grant agreement No 754303.

We acknowledge the Agence Nationale de la Recherche under the programs "Investissements d'avenir" (ANR-15-IDEX-02), and CMOSQSPIN (ANR16-ACHN-0029).

We acknowledge the support of European Union's Horizon 2020 research and innovation actions (RIA) project SEQUENCE under Grant Agreement No. 871764.

The institute state-of-the-art equipment is co-financed by the Auvergne Rhône-Alpes region.



ABOUT CEA-LETI (FRANCE)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro- & nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 3,100 patents, 10,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo. CEA-Leti has launched 69 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Technological expertise

CEA has a key role in transferring scientific knowledge and innovation from research to industry. This high-level technological research is carried out in particular in electronic and integrated systems, from microscale to nanoscale. It has a wide range of industrial applications in the fields of transport, health, safety and telecommunications, contributing to the creation of high-quality and competitive products.

For more information: www.cea.fr/english

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