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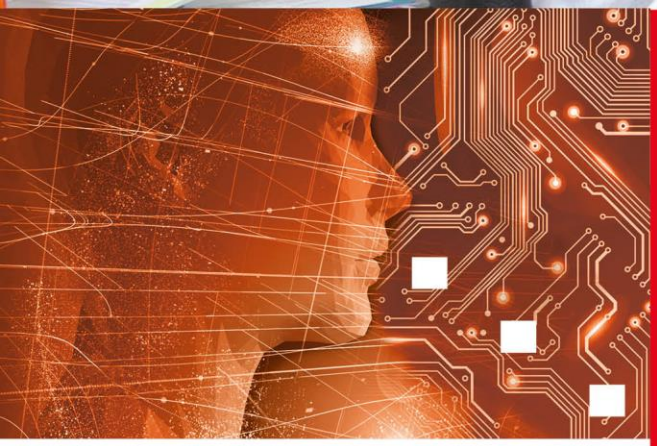


SILICON TECHNOLOGIES AND COMPONENTS

ANNUAL
RESEARCH REPORT
2018

leti
cea tech

TECHNOLOGY
RESEARCH
INSTITUTE

Committed to Innovation, Leti Creates Differentiating Solutions for its Industrial Partners.

Leti is a research institute of CEA Tech and a recognized global leader in miniaturization technologies. Leti's teams are focused on developing solutions that will enable future information and communication technologies, health and wellness approaches, clean and safe energy production and recovery, sustainable transport, space exploration and cybersecurity.

For 50 years, the institute has built long-term relationships with its industrial partners, tailoring innovative and differentiating solutions to their needs. Its entrepreneurship programs have sparked the creation of 64 start-ups. Leti and its industrial partners work together through bilateral projects, joint laboratories and collaborative research programs.
Leti maintains an excellent scientific level by working with the best research teams worldwide, establishing partnerships with major research technology organizations and academic institutions. Leti is also a member of the Carnot Institutes network*.

*Carnot Institutes network: French network of 34 institutes serving innovation in industry.

DE LA RECHERCHE À L'INDUSTRIE
cea

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in research, development and innovation in defense & security, nuclear energy, technological research for industry and fundamental physical and life sciences.

www.cea.fr/english

Leti at a glance

€315
million budget

800
publications per year

ISO 9001
certified since 2000

Founded in
1967

Based in
France (Grenoble)
with offices in the
USA (Silicon Valley)
and **Japan** (Tokyo)

350
industrial partners

1,900
researchers

2,760
patents in portfolio

91,500
sq. ft. cleanroom space, 8" & 12" wafers

64
startups created

SILICON TECHNOLOGIES AND COMPONENTS

Within CEA Tech and Leti, silicon technologies and components research activities are shared between two divisions gathering together around 600 researchers:

The Silicon Technologies Division carries out innovative process engineering solution and research, operates 24/7 year round, 7500m2 of state-of-the-art cleanroom space divided into three different technology platforms.

The Silicon Components Division carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend Moore's Law for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.

This booklet contains 48 one-page research summaries covering advances in the focus areas of our Silicon Devices and Technologies Divisions, highlighting new results obtained during the year 2018.

CONTENTS

EDITO

Laurent Clavelier,
Head of Technological platforms

Dear Reader,

2018 was a very rich year in terms of results, investments and organization. It was the year we decided to launch our ambitious plan for 300mm technology autonomy for the CEA-LETI. This investment plan covers a period of 4 years.

Starting in 2018, we acquired a new lithography capability with a 193mm immersion scanner. Today this scanner is in operation and performing advanced lithography since October 2018 on CMOS, memories and photonic demonstrators. The next step of the plan is in progress with a focus on tools that are essential for ST and SOITEC programs: substrates, nonvolatile memories and imagers.

All this infrastructure and associated programs are important for our scientific activities. Since 300mm tools are the most advanced in term of performances, they are unique in allowing us to explore new areas and phenomena with the ability to integrate directly on real devices. To do that, a strong scientific understanding, and thus strong scientific positioning, is mandatory.

In terms of scientific results, I would like to thank our teams for their impressive achievements: 100 abstracts accepted at international conferences; 100 peer reviewed journal papers accepted; 9 ANR and 6 EU projects submitted to support our most advanced activities. We have also generated 42 patents.

Epitaxy of IV, II-V and II-N materials, CMP, molecular bonding, advanced and alternative lithography (nanoimprint, DSA), 2D materials, materials for nonvolatile memories, advanced metrology and characterization, … are some of the domains in which we are strongly involved and in which we will reinforce our activity. All this is possible because we collaborate with our colleagues from the applicative divisions and academic laboratories in France (CEA fundamental research, CNRS-LTM, IEMN, CEMES, …) but also in the EU and across the world (FhG, IMEC, Stanford, Caltech, …).

To finish, I would like to welcome a new activity to our division: material and technology activities for photonics (II-VI and III-V) have just joined us in January 2019. The scientific activity and knowledge of these laboratories rely on a solid and long term expertise. Thus, cross fertilization with IV material activities are expected in 2019!

EDITO

Pascale Berruyer,
Head of Silicon Components

Dear Reader,

Today, societal needs in terms of wellness, mobility, communication, and ubiquitous services are driving the rapid evolution of microelectronic technologies. High performance computing, advanced RF communications, power electronics and advanced sensors are key elements for AI, 5G communications, IoT, autonomous driving, hybrid and electrical vehicules. With the central mission to efficiently develop the related advanced hardware, the Silicon Components Division is at the heart of all these societal demands, broadly relying upon state-of-the-art 300 and 200 mm facilities. These facilities allow our experts to continuously assess disruptive technologies and federates global partnerships for an efficient industrial manufacturing of these solutions. Significant successes have been achieved in 2018 in the fields of advanced nanoelectronics, power electronics and sensors.
Just to highlight few of them, let me mention:
-the important Léti support to industrialization of FDSOI which has now reached its maturity.
-the achievement of major breakthroughs in 3D sequential technology CoolCubeTM.
-the rise of quantum activities in partnership with CEA-INAC and Néel institute, and particularly the implementation of a technology platform mixing Qbits devices and CMOS electronic control. An ERC Synergy grant has just been obtained to also support this activity.
-the collaboration with STMicroelectronics Crolles to develop next generations of PCM embedded non-volatile memories addressing automotive and smartcard markets.
-the increasing partnership with STMicroelectronics Tours and Catane through IRT/Nanoelec and IPCEI-Nano2022 programs on diodes and power transistors on GaN on Si, with a maturity 10 achieved on 650V diodes.
-the implementation of new concepts for environmental and biological sensors, especially based on optomechanical nanoresonators.

It is worth noting that most of the highlighted successes have been achieved in the frame of outstanding bilateral partnerships and with the sustained efforts of our team that I would like to sincerely thank here.

I hope you will enjoy reading the overview of these achievements.

EDITO

Jean-Charles Barbé & Raluca Tiron
Chief Scientists

We are proud to release our eighth Silicon Components and Technologies Annual Scientific Research Report, for the year 2018. This booklet contains 48 one-page research summaries covering advances in the focus areas of our Silicon Components and Technologies Divisions, highlighting new results during the year.

The year 2018 illustrates the continuing innovation of our Si technologies divisions to contribute from a hardware point of view to the big data and artificial intelligence area, Internet of Things (IOT), automotive, energy, health and environment monitoring.

In this annual report, we confirmed our positioning in disruptive Si research with several highlights including quantum computing development on Si CMOS, neuromorphic architecture with emerging resistive memories, reduced programming consumption in RRAM arrays, innovative back-end selectors for memories, disruptive 3D concept or advanced mask-less pattering, opto-mechanic resonators, RF switches concepts with emerging materials, advanced GaN-on-Si for power electronics.

Our research on future IoT sensing systems includes new transducers, embedded RF functionalities and substrates, embedded intelligence, dedicated packaging, energy harvesters and micro-batteries.

In 2018, the Silicon Divisions produced 403 publications, achieving impact factors as high as 41.

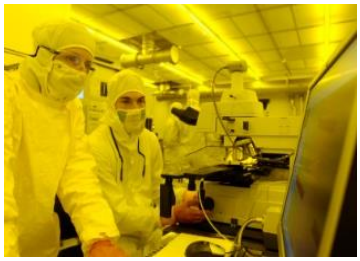
We thank our industrial partners for their continuing confidence in us. We are committed to ensuring the transfer of the most advanced research to industry. Strong industrial partnerships are the foundation of our culture of innovation.

We are committed in international scientific collaborative research by participating in major european research programs, European Research Council grants, international conferences, program committees, boards of governors and evaluation committees.

Underlying all these efforts is the cooperation of all our researchers and management, as well as the Silicon Technologies and Components Divisions and CEA-LETI's scientific advisory board.

We also wish to extend my appreciation to the 11 chapter's editors and authors of the 2018 Scientific Report, who spared no effort to prepare this document.

KEY FIGURES



498 researchers

135 industrial residents

498 PhD students in 2018

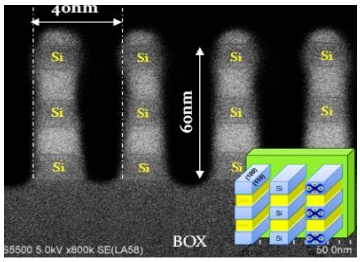
12 Post-docs in 2018

200 & 300 mm platforms for advanced CMOS/3D

250 tools for 200 mm, non stop operation

140 tools for 300 mm, non stop operation

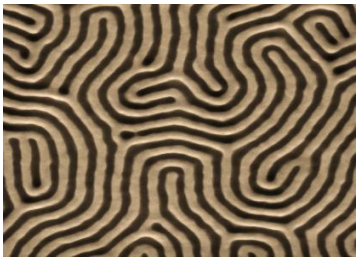
6100 m² cleanroom ISO3-5



200 mm platforms for MEMS

130 tools, non stop operation

2200 m² cleanroom ISO4-



122 commun laboratories

124 patent filed in 2017

403 papers issued in 2017 (WOS, SCOPUS)

TECHNOLOGICAL PLATFORMS

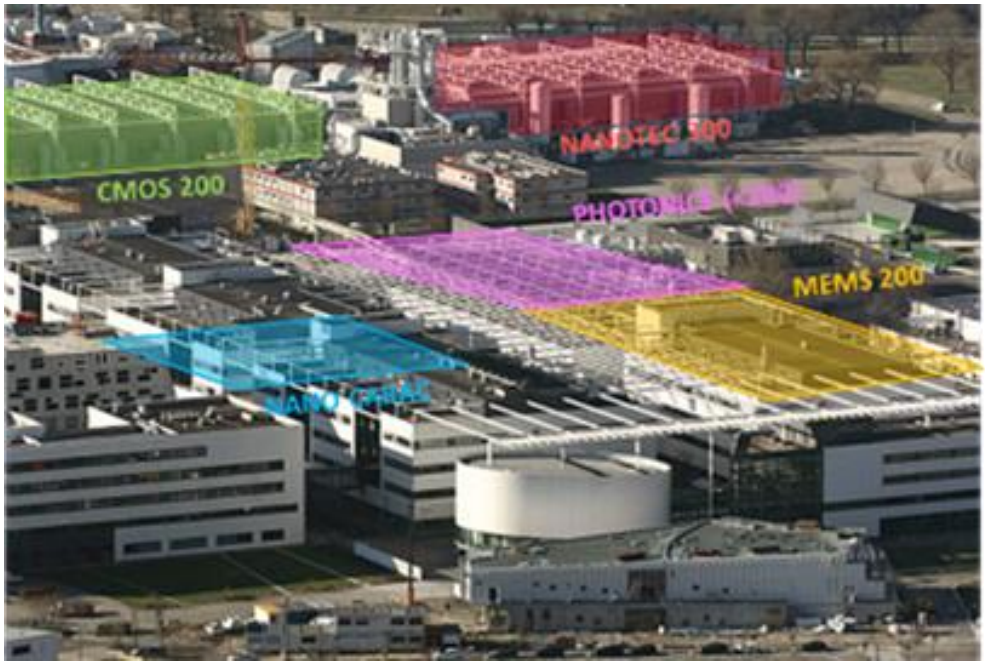
The silicon divisions operate 8300 m² of state-of-the-art cleanroom space divided into three platforms, gathering 500 process tools and a combined staff of more than 450; they run industry-like operations, 24 hours a day, 7 days a week, all year round.

- The 300 platform provides 300mm wafer processing, which can be applied to both semiconductor and microsystem devices.
- The 200mm platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS).

Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system links the two platforms to add process flexibility and faster processing.

- The multi-scale platform for imagers and IR applications.

All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers eight domains of competencies, including electron microscopy, X-ray diffraction, ion beam analysis, optics, scanning probe, surface analysis and sample preparation, magnetic resonance.



ORGANIZATION

Silicon Technologies Division is organized according to six departments.

- Three Process Departments whose missions are to execute generic process steps for all projects and to develop innovative processes to provide state-of-the-art solutions to internal and external customers. These departments are focused on patterning, deposition, and surface treatments. Their research activities in collaboration with key universities will support Leti's advanced position in the future.
- A Characterization Department whose mission is to perform off-line observations to characterize process steps, materials or components. This department also has a research activity to maintain its level of excellence.
- Two Support Departments: one is in charge of the planning, the interface with internal divisions or external customers as well as methods, training and clean-concepts. The other is responsible for facilities operations and engineering.
-

Silicon Components Division is organized around three departments with clear objectives and market focus.

- Memory and compute mission is to simulate, model, develop, demonstrate and test new generations of circuits and modules for sub-20nm CMOS, digital and memory.
- Sense and Act Department designs and develops innovative microsystem components (sensors, actuators) and the associated toolbox (packaging, heterogeneous integration, reliability).
- Power Energy and Connectivity Department develops and demonstrates technology modules and components for power and energy (photovoltaic, power electronics, RF, integrated storage)

SCIENTIFIC ACTIVITY

Publications

178 publications in 2018 (WoS, SCOPUS)

225 international conference communications.

Prize and awards

G. Poupon, 2018 IEEE EPS Regional Contributions Awards

M. Kazar Mendes, Best Poster Award EMRS, Spring meeting 2018

M. Moreno Villavicencio , Best Student Award, AVS 65th, 2018

J.M. Hartmann, ECS Appreciation Award, AIMES 2018

M. Mastari, Best student paper award, ECS Cancun Oct. 2018

F. Andrieu, Prix Brillouin-Glavieux 2018

A. Verdy, Best student paper award IMW 2018

R. Alhalabi, Best poster award, NVMTS2018

V.Enyedi, Best poster award. Spectratome 2018

2 on-going European Research Council Grants (S. Hentz, D. Cooper)

2 newly-started European Research Council Grants (F. Andrieu, M. Vinet)

- Experts

7 International Experts,
4 Research Directors,
38 Senior Experts,
56 Experts,
26 of them holding an HDR.

Scientific committees

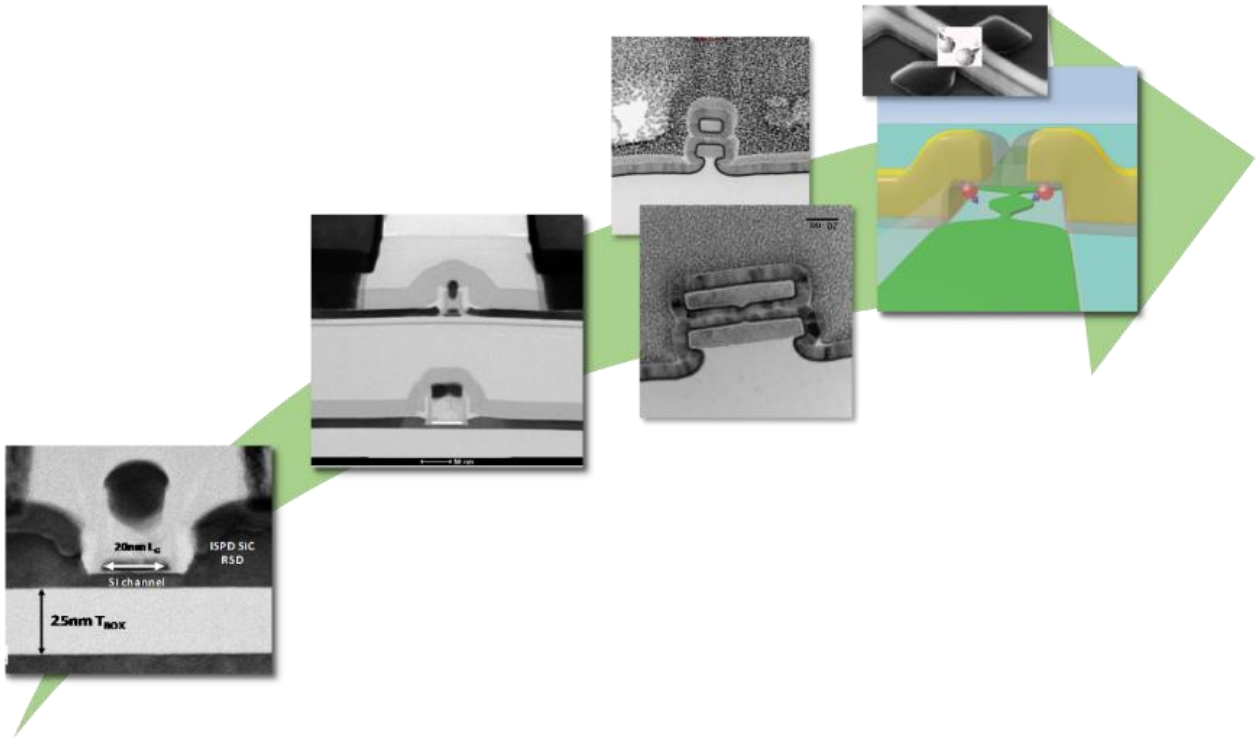
• National Research Agency committee.
• Technical Program committees of:
IEEE-IEDM, IEEE-VLSI, IEEE S3S,
IEEE ESSDERC, IEDM
IEEE-IITC, MAM
ECS AIMES – SiGe symposium
ECS AIMES – Bonding symposium
SPCC, ICSI-ISTDM,ICPT
ICMOVPE, Waferbond
AMC, ECS Transactions AIMES,
JNTE, AVS, SPIE Advanced Lithography,
SISC, SSDM, ICICDT, MRS, IMW
Scientific comitee for (Collaborative Research Group) Françaises de l'ESRF

Conferences and Workshops organizations

G03 SiGe Symposium at AIMES,
DSA Symposium,
PESM,
2nd workshop of the European FIB Network

International Collaborations

Forschung Zentrum Juelich (Germany),
Stanford University (USA),
Caltech (USA),
The University of California (USA),
Fraunhofer institutes (Germany),
Università degli Studi di Ferrara (Italy)
University of Cambridge (GB),
Université Catholique de Louvain (Belgium),
Politecnico Di Milano (Italy),
Paul Scherrer Institute (Switzerland),
École Polytechnique Fédérale de Lausanne (Switzerland), ETH – Zürich (Switzerland),
CNR (Italy),
University of Chicago (USA),
Sherbrooke, University (Canada)
NIMS (Japan),
University of Southern Denmark
University Cagliari (Denmark),
Institute for Technical Physics and Materials Science (Budapest),
Hungarian Academy of Sciences (Budapest),
Korea University (Seoul)
Centro universitario FEI (Brazil),
University of Tsukuba (Japan).


20nm L_G
ISPD SiC
RSD
Si channel
25nm T_{BOX}

O1 CORE & BEYOND CMOS

- **Integration of Spin Quantum Bits in Silicon MOS Technology**
- **Breakthroughs in 3D Sequential Technology**
- **Towards a High Performance and Reliable 3D Sequential Integration**
- **Low Temperature Epitaxy and Clean for CoolCube™ Integration**
- **Advanced FDSOI CMOS: Strain Optimization and Design Technology co-Optimization**
- **Recent Bulk Modelling Development on PSP Model and Prospective Modeling of Single Event Transients.**
- **Strain Maps And Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets FETs**

Integration of Spin Quantum Bits in Silicon MOS Technology

RESEARCH TOPIC:

Quantum information, spin, qubits, silicon, CMOS

AUTHORS:

Louis Hutin, Benoit Bertrand, Vincent Mazzocchi, Jean-Michel Hartmann, Maud Vinet (Yann Michel Niquet, Tristan Meunier)

ABSTRACT:

We fabricated Si Quantum Dot (QD) devices using relatively minor adaptations of a standard SOI CMOS process flow. We demonstrated that the spin of confined charges could be controlled via a local electrical-field excitation, owing in the case of electrons to a geometrically-enabled tuning of the valley splitting and inter-valley spin-orbit coupling. Furthermore, we investigated improvement paths such as extending the spin coherence time by using epitaxially-grown layers of nuclear-spin-free ^{28}Si (99.992%) as a device template, and developing novel 3D architectures compatible with topological quantum error correction schemes.

SCIENTIFIC COLLABORATIONS: CEA-IRIG, CNRS Institut Néel

Context and Challenges

We aim to engineer devices for the coherent manipulation of information encoded as a quantum superposition of basis states, *i.e.* quantum bits (qubits). In particular, the qubit state is mapped to the spin of a charged particle confined in a Quantum Dot (QD). In our case, holes or electrons are accumulated below MOS Gates wrapping around mesa-etched Si NanoWires (NW), forming 1D arrangements of nearest neighbor-coupled QDs. Coherent control and dispersive readout of hole spin qubits were recently demonstrated in such CMOS-compatible devices. We continue to explore ways to improve quantum information fidelity through developing control schemes, material engineering and architectures.

Main Results

Surprisingly, we observed spin transitions in MOS Gate-confined electrons using only E-field excitations. The underlying mechanism is based on the interplay between Spin-Orbit Coupling (SOC) and the multi-valley structure of the Si Conduction Band, and is enhanced by the "Corner QD" device geometry. We also showed that by offering the ability to break and restore the confinement symmetry at will, the SOI Back-Gate may allow fast programming in valley mode, and stable information storage in spin mode [1]. This functionality could alleviate the trade-off between fast manipulation and long coherence time, thereby improving the outlook for compact, scalable and fault-tolerant quantum logic circuits.

Hyperfine interactions with nuclear spins in the host crystal can limit the coherence time of an electron spin qubit. The most abundant Si isotope (^{28}Si: 92.23%) carries no nuclear spin, but ^{29}Si (4.67%) does. We have grown epilayers with a ^{28}Si isotopic purity greater than 99.992% on 300 mm diameter natural abundance silicon (^{nat}Si) crystals (Fig. 1). The quality of the mono-crystalline isotopically purified epilayer conforms to the same drastic quality requirements as the natural epilayers used in our pre-industrial CMOS facility [2].

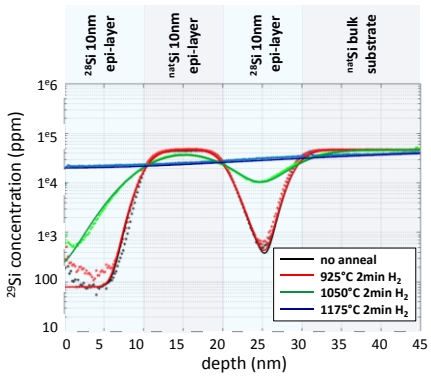


Figure 1: SIMS data (symbols) and simulation results (lines) of ^{29}Si concentration depth profile vs. annealing conditions in a ^{28}Si 10nm / ^{nat}Si 10nm / ^{28}Si 10nm / bulk ^{nat}Si stack [2].

Perspectives

Motivated by topological compatibility with Quantum Error Correction (QEC) codes, disruptive architecture proposals have emerged recently, relying on crossbar addressing of 2D arrays of QDs. Our own 3D architecture (Fig. 2) features a large 2D array of Si QDs with line/column control of their tunnel coupling to the nearest neighbors. It is also coupled to a lower tier of Si QDs enabling fast initialization and readout.

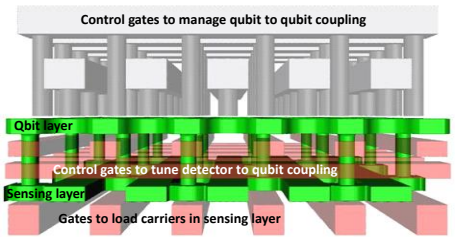


Figure 2: 3D architecture for Quantum Error Correction [3].

RELATED PUBLICATIONS :

[1] L. Hutin et al., VLSI Tech. Symp. 2018, 10.1109/VLSIT.2018.8510665
[2] V. Mazzocchi et al., J. Crystal Growth, 2018, 10.1016/j.jcrysgro.2018.12.010
[3] M. Vinet et al., IEDM 2018, 10.1109/IEDM.2018.8614675

Breakthroughs in 3D Sequential Technology

RESEARCH TOPIC:
3D sequential, CoolCube, low thermal process, gate stack, iBEOL, Smart Cut

AUTHORS:
C. Fenouillet-Beranger, L. Brunet, P. Batude, N. Rambal, F. Ponthenier, E. Arnoux, F. Andrieu, M. Vinet (J. Aubin, J-B. Pin)

ABSTRACT:
The 3D sequential integration, of active devices requires the thermal budget of top tier processing to be limited to 500°C in order to ensure the stability of the bottom devices. Here we present breakthroughs in six areas that were previously considered as potential showstoppers for 3D sequential integration from either a manufacturability, reliability, performance or cost point of view. Our experimental data demonstrate the ability to obtain 1) low-resistance poly-Si gate for the top FETs, 2) Full low-temperature RSD epitaxy 3) Stability of intermediate BEOL (iBEOL), 4) Stable bonding above ULK, 5) Efficient contamination containment for wafers with Cu/ULK iBEOL enabling their re-introduction in FEOL for top FET processing 6) Smart Cut™ process above a CMOS wafer.

SCIENTIFIC COLLABORATIONS: STMicroelectronics (France), AMAT (France), SCREEN-LASSE (France)

Context and Challenges
3D-monolithic or 3D sequential CMOS technology is based on stacking active device layers on top of each other with very small 3D contact pitch (similar pitch as standard contact). However, such an integration process faces the challenge of fabricating high-performance devices in the top tier without degrading the electrical characteristics of the bottom tier. Therefore, limiting the thermal budget to 500°C is mandatory. Owing to in-depth and exhaustive experimental studies, our previous work has highlighted two critical processing issues: i) Low-temperature gate stack integration ii) Low-temperature selective epitaxy of silicon on source and drain. In parallel we recently demonstrated for the first time the integration of low temperature SiCO spacer material deposited at 400°C in both standard (High temperature) and low temperature (LT) anneal CMOS FDSOI process flow [1]. This work presents advances bringing 3D sequential integration closer to manufacturability. Here we present six achievements on process steps that were considered as potential showstoppers for this technology (Fig.1).

Main Results
In order to obtain high performance top FETs, low gate access resistance has been achieved using UV nano-second laser recrystallization of in-situ doped amorphous silicon [2]. Full 500°C selective Si epitaxy process is demonstrated owing to an advanced LT surface preparation with a combination of dry and wet etch preparation; the selective epitaxial growth is obtained with the cyclic use of a new Si precursor and Cl2 etching.
In parallel, this work paves the way to manufacturability of 3D sequential integration including iBEOL with standard ULK and Cu metal lines. A bevel edge contamination containment strategy composed of 3 steps (bevel etch, decontamination, encapsulation) enable wafers re-introduction in FEOL environment after BEOL process. In addition, the stability of line to line breakdown voltage for interconnections submitted to 500°C anneals is demonstrated for the first time.

Finally, Smart Cut™ transfer of a crystalline silicon layer on a processed bottom level of FDSOI CMOS devices is demonstrated as an alternative to SOI bonding and etch back process scheme for top channel fabrication (Fig.2).

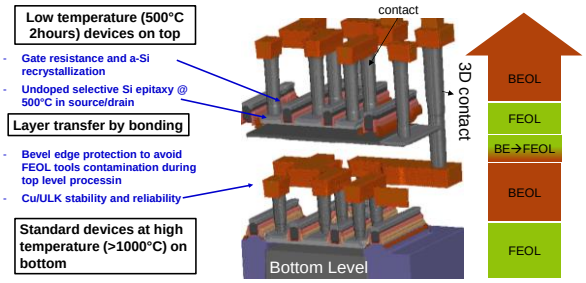


Figure 1: 3D sequential Coolcube™ integration and remaining process issues.

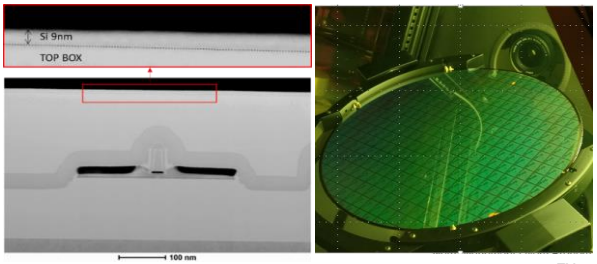


Figure 2: STEM cross-section after layer transfer by Smart Cut™ process and thinning above a 20nm gate length transistor (left). The corresponding photography of layer transfer above CMOS.

Perspectives
A full low temperature 500°C devices integration is ongoing for the top level of the CoolCube™ integration.

RELATED PUBLICATIONS:
[1] C. Fenouillet-Beranger et al., SSDM, 2018, https://confit.atlas.jp/guide/event/ssdm2018/subject/B-6-02/advanced
[2] L. Brunet et al., IEEE IEDM, 2018, 10.1109/IEDM.2018.8614653

Towards a High Performance and Reliable 3D Sequential Integration

RESEARCH TOPIC:

3D sequential integration, low thermal budget process flow, transistor reliability

AUTHORS:

X. Garros, A. Tsiara, L. Brunet, P. Batude, C. Fenouillet-Béranger (G. Ghibaudo)

ABSTRACT:

LETI demonstrates not only great performance but also excellent reliability of a 3D sequential integration scheme. We highlight, for the first time, that the top level transistor can be successfully processed at 630°C with almost no impact on the performance and reliability of the bottom level. Key properties of the gate stack like EOT and leakage current are preserved as well its immunity to trapping. We also prove that these top level devices made at low temperature can already meet key reliability requirements as DC 5 years BTI lifetime. Finally an example of successful and robust 3D logic integration is proposed based on a 3D inverter combining a top-level PMOS with a bottom-level NMOS. This work gives pathways towards a reliable 3D sequential technology.

SCIENTIFIC COLLABORATIONS: IMEP-LAHC

Context and Challenges

3D Sequential CoolCube™ integration is based on stacked layers of devices fabricated one on top of each other, allowing extremely scaled 3D contact pitch [1]. However the fabrication of the two level transistors faces many integration challenges. Amongst them, reliability remains a key issue. Actually the top transistor must be processed at low temperature in order to preserve the integrity of bottom level MOSFET and BEOL levels. However, using a low thermal budget may reduce the top device performance by increasing access resistance and/or decreasing channel carrier mobility. It may be also detrimental for the gate oxide reliability because the curing of microscopic defects responsible for trapping is less effective at lower temperature. However, it is still unclear if a 3D sequential integration can be reliable enough since, so far, no study has addressed the reliability concern in a true 3D sequential technology.

Main Results

The purpose was therefore to propose an in-depth analysis of both performance and reliability of a 630°C fully integrated 3D sequential technology. An example of a 3D integration is shown in Fig. 1 through a two level CMOS inverter.

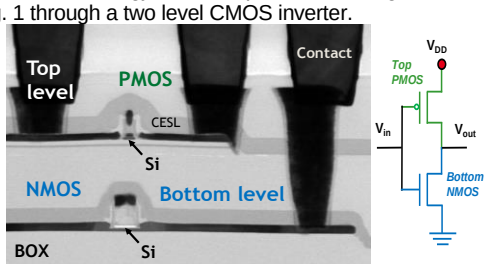


Figure 1: Cross-sectional TEM image of 3D inverter made of a bottom level NMOS and a top level PMOS.

The objectives of this work were twofold (1) to address how the top level processing impacts the performance and reliability of the bottom one (2) to assess the intrinsic reliability of the top level device processed at 630°C; a much lower temperature than for a conventional gate first integration process T>1000°C. To investigate (1), we compared the BTI reliability of bottom level transistors, which have seen the process of the top level, to the one of simple planar 2D references (only ground level, no level on the top). For BTI (see Fig.2) as well as for Hot Carrier (not shown here), no difference is visible between both kinds of devices. This clearly demonstrates that the gate oxide quality of the bottom level devices is not altered by the top level processing at 630°C. For (2), we compared the BTI lifetime of Bottom and Top level NMOS and PMOS devices (see Fig. 3). Even if PBTI is slightly degraded for top level devices, the BTI requirements -VG for 5 years working must be over 0.95V - are met for both bottom and top transistors. This is a first demonstration that 3D sequential technology can reach the reliability standards for digital CMOS applications [2].

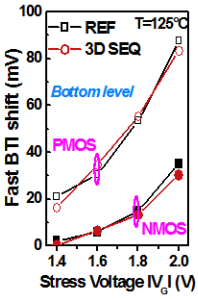


Figure 2: Impact of top level processing on BTI reliability of the bottom level transistor.

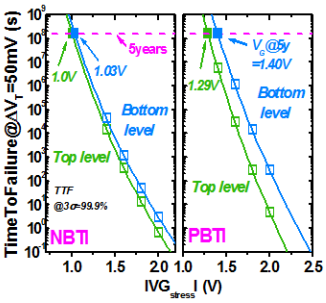


Figure 3: Extraction of BTI lifetime for bottom and top level transistors. BTI lifetime Is over 5 years in all cases (>V_{DD}+5%=0.95V)

Perspectives

The key challenge will be now to reduce the temperature of the top level process below 600°C while keeping the same quality of the top transistor gate oxide. This is required to cope with all the possible applications targeted by this technology.

RELATED PUBLICATIONS:

[1] L. Brunet et al., Electrochemical society spring meeting, Seattle, 2018, 10.1149/08508.0125ecst

[2] A. Tsiara et al., Proceedings of IEEE Symposium on VLSI Technology, 2018, 10.1109/VLSIT.2018.8510625

Low Temperature Epitaxy and Clean for CoolCube™ Integration

RESEARCH TOPIC:
Low temperature Si and SiGe selective epitaxy, Siconi surface preparation, CoolCube™ integration

AUTHORS:
V. Mazzocchi, P.E. Raynal, V. Loup and J.M. Hartmann
(P. Besson, J.B. Pin)

ABSTRACT:
The features of Metal Oxide Semiconductors Field Effect Transistors (MOSFETs) become smaller and smaller in advanced technology nodes, with a clear switch from planar to 3D devices such as finFETs or stacked nanosheets. Monolithic 3D integration, i.e. Coolcube™, is definitely an option in order to increase the density of devices per footprint. It consists in stacking layers of transistors on top of one another, with definite constraints concerning the thermal budget used for top device fabrication (it should be low in order not to degrade the performances of the bottom devices). We are evaluating various strategies in order to minimize the temperature used during (i) surface preparations and (ii) epitaxial growth processes, which should be selective against dielectrics, 500°C being the targeted value.

INDUSTRIAL COLLABORATIONS: AMAT, STMicroelectronics

Context and Challenges
Low temperature selective epitaxy is of paramount importance in order to (i) thicken the Source and Drain regions of top level Metal Oxide Semiconductor Field Effect Transistors without degrading the properties of bottom MOSFETs (in monolithic 3D integration), (ii) encapsulate small 3D objects such as fins without altering their shape and so on.
Such processes consist in a surface preparation (made of a wet cleaning, potentially an in-situ NH_3/NF_3 remote plasma Siconi™ process and an in-situ H_2 bake) followed by the growth itself, which can occur in a single step (with chlorinated gaseous precursors, usually) or through an alternating between non-selective growth steps (with hydrogenated precursors) and selective etch steps (with HCl or Cl_2). In the following, we will show some of the results we have obtained on (i) the impact of a Siconi™ process on the surface preparation of Si and SiGe and (ii) the low temperature growth kinetics of Si and SiGe with mixtures of conventional gaseous precursors or liquid Si.

Main Results
We have evaluated in Ref. [1] the interest of using an *in-situ* Siconi™ process, which transforms native or chemical oxides into salts which can be sublimated at low temperatures, avoiding thereby surface re-oxidation during wafer transfer. On Si surfaces, we succeeded in reducing by 25°C the threshold H_2 bake temperature above which there are no interfacial oxygen peaks anymore (see Fig. 1 (top)). We otherwise obtained much lower O interfacial contamination at temperatures less than 750°C, which has an impact on epitaxial quality. We also showed that *ex-situ* wet cleanings creating SiO_2-rich chemical oxides followed by Siconi™ processes yielded smooth SiGe surfaces free of any oxide.
We have investigated in Ref. [2] the impact Si precursor mixing has on the Si and SiGe growth kinetics in the 500°C-575°C range, with far from straightforward trends observed. We have otherwise benchmarked, for the same purpose, a liquid Si precursor against disilane. Significantly higher growth rates for a given Ge concentration were obtained with the former at 500°C, as shown in Fig. 1 (bottom). Reasonable Si growth rates were achieved with liquid Si at temperatures as low as 475°C, i.e. 75°C lower than with silane (SiH_4), for instance.

Perspectives
The fitness of the sequence proposed for SiGe surface preparation is being evaluated through the re-epitaxy of SiGe on top, with interesting trends emerging. Liquid Si is being used in non-selective growth steps together with Cl_2 selective etch steps to fabricate Si raised sources and drains at 500°C.

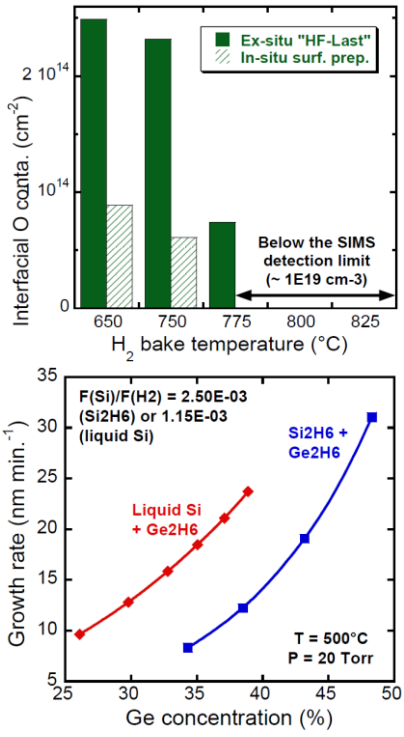


Figure 1: (top) interfacial O contamination (in Si) as a function of the H_2 bake temperature after "HF-Last" or Siconi™ surface preparations (bottom) Growth rate versus Ge concentration for different chemistries, showing the interest of using liquid Si.

RELATED PUBLICATIONS:
[1] J.M. Hartmann et al., ECS Transactions 86 (7) 219, 2018, 10.1149/08607.0219ecst
[2] V. Mazzocchi et al., ECS Transactions, 86 (7) 177, 2018, 10.1149/08607.0177ecst

Advanced FDSOI CMOS: Strain Optimization and Design Technology co-Optimization

RESEARCH TOPIC:
FDSOI, DTCO, strain, Body biasing, Local Layout Effect

AUTHORS:
F. Andrieu, C. Fenouillet-Beranger, O. Weber, M. Vinet, R. Berthelon, D. Rouchon, G. Cibrario, B. Giraud

ABSTRACT:
Performance/Power/Area of CMOS digital circuits on next-node FDSOI can be improved by strain optimization and Design/Technology Co-Optimization (DTCO). LETI has carried out studies to measure the strain by Raman for different CMOS process integration schemes in order to optimize the performance. Moreover, DTCO was carried out in SRAM leading to an innovative Complementary SRAM design using SiGe channel in the pass-gate. Finally, for standard cells, we propose an original Technology/Design Co-optimization, mixing devices of different threshold voltages (V_T-flavors) within a cell. It enables adjusting the V_T of pMOS subject to SiGe channel-induced Local Layout Effect (LLE); leading experimentally to a 23% frequency gain on 22nm FDSOI technology for a 2-finger inverter Ring Oscillator (IVSX2 RO) vs. reference LVT at the same static leakage and V_{DD}=0.4V supply voltage; which corresponds to the Minimum Energy Point (MEP). This solution is combined with Forward Body Biasing (FBB).
SCIENTIFIC COLLABORATIONS: STMicroelectronics (France), Globalfoundries (Dresden, Germany)

Context and Challenges

FDSOI CMOS offers an excellent performance/power/cost tradeoff for mobile, IoT and wearable applications. Moreover, its excellent electrostatic control and variability, as well as its back-bias capability, make it a good candidate for Ultra-Low-Voltage (ULV) operations. Performance/Power/Area tradeoff can be optimized for next FDSOI by strain optimization and Design/Technology Co-Optimization (DTCO).

Strain optimization

We fabricated SiGeOI by the Ge-enrichment process and SiGe/SOI bilayer by epitaxy. On these materials, nanosheets were patterned down to 100 nm width and characterized by µRaman spectroscopy for different CMOS process integration schemes. We evidence experimentally a relaxation of the compressive strain in SiGe for narrow lines, which is higher for SiGeOI than for SiGe/SOI at W=500 nm, in qualitative agreement with the electrical results we measured on planar FDSOI pMOSFETs. We highlight the interest of a tensile nitride capping on top of SiGe in order to maintain the stress during active patterning and demonstrate that a 0.45% tensile stress could be generated in 100 nm narrow stripes in the underneath SOI layer of the SiGe/SOI bilayer [1].

DTCO in SRAM

We investigated the introduction of an SiGe channel in FDSOI SRAM bitcells by the means of spice simulation. In classical SRAM configuration performance (read, write, retention) at a given leakage is only slightly impacted because of the SiGe stress partial relaxation in the small Pull-Up active dimensions. Since the SiGe compressive stress strongly enhances the hole mobility for long active stripes, it is relevant to design a so-called Complementary-SRAM bitcell, using SiGe pFETs as both Pull-Up and Pass-Gate devices. In such an innovative configuration, the read current is enhanced by +21% with respect to the reference at the same leakage.

DTCO in standard cells

Local Layout Effect (LLE) induced by SiGe-channel impacts the device centering in advanced FDSOI technologies. Process or (continuous-RX) design solutions exist to suppress LLE and get the maximum performance from the SiGe booster. We have proposed an original design that mitigates SiGe-induced LLE to increase the performance while preserving low-leakages. It consists in mixing within a standard cell different V_T flavors (Fig.1). Some 22FD-SOI ULV features were measured on inverter ROs: Minimum Energy Point (MEP) below 0.4 V and min Energy-Delay-Product (EDP) at V_{DD}≈0.65 V for LVT. We show also for the first time that an optimum V_B exists leading to -13% min EDP (vs. V_B=0) (Fig.2). On these ULV cells using within-cell V_T-mixing, leads to +23% frequency for IVSX2 vs. ref LVT at the same static leakage and V_{DD}=0.4 V (Fig.3).

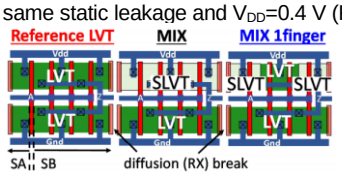


Figure 1: Schematic of LVT, MIX and MIX 1finger cells.

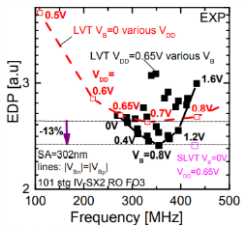


Figure 2: EDP vs. frequency for LVT V_B=0 (various V_{DD}) and at V_{DD}=0.65V (various V_B). Lines correspond to $|V_{Bn}|=|V_{Bp}|$

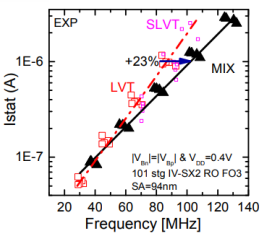


Figure 3: Istat vs. frequency for LVT, SLVT and MIX

Perspectives

FDSOI is an attractive technology for IoT, edge-IA, RF applications. 28 nm, 22 nm and 12 nm CMOS platforms exist in the industry and solutions for sub-12 nm have been developed at LETI.

RELATED PUBLICATIONS:
[1] R. Berthelon et al., SSDM, 2018; https://confit.atlas.jp/guide/event/ssdm2018/subject/C-3-02/date?cryptoId=
[2] F. Andrieu et al., IEEE VLSI Symposium, 2018, 10.1109/VLSIT.2018.8510636
[3] R. Berthelon et al., EuroSOI, 2018, 10.1109/ULIS.2018.8354730

Recent Bulk Modelling Development on PSP Model and Prospective Modeling of Single Event Transients.

RESEARCH TOPIC:
PSP, Single Event Transients, Compact model, SPICE, Bulk transistor

AUTHORS:
S. Martinie, O. Rozeau, N. Rostand, J. Lacord, T. Poiroux, J-C. Barbé (André Juge, Geert D. J. Smit, G. Hubert)

ABSTRACT:
With the maturity of CMOS technologies and their use for low voltage analog applications, some additional parasitic effects must be modeled to improve the accuracy of SPICE models. This paper describes the latest significant improvements of PSP bulk MOSFET model including new compact models of parasitic MOSFET and interface states. We also presented our recent work on Single Event Transients (SET) which are important issues concerning reliability. They lead to occurrence of soft errors in integrated circuits, such as Single Event Upset (SEU), which consists in unexpected bit state switch in SRAM cells. Here, we describe the implementation in Verilog-A of a new approach and use it to study the effect of SET on SRAM cell.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, NXP Semiconductors, ONERA.

Context and Challenges

PSP is a standard compact model for deep-submicron bulk Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). Since 2015, CEA-LETI is the main developer of PSP and continues to improve accuracy in-line with industrial expectations. Especially, with the decrease of supply voltage, devices operate close to the weak inversion, where some effects such as parasitic sidewall transistor, and the interface states effect, can have a significant impact. On the other hand, the effect of natural radiations (neutrons …) on CMOS circuits has been widely demonstrated and are even more significant as we decrease transistor sizes. SET are one of these effects and consist in the formation of parasitic current pulses within MOSFETs after the particle impact. Here, we explore new ways of modeling development to include the SET effect into the compact model formalism.

Main Results

Fig. 1.a & b represents different figures of merit on current and gm versus gate voltage for different values of back gate voltage and two geometries (large W=L=10 µm and narrow W=0.5 µm L=10 µm transistor). The hump induced by the parasitic transistor is well reproduced by the proposed model even for narrow transistors, where the parasitic transistor is predominant on total current as highlighted on gm of figure 1.b.
The influence of non-uniform related DIT parameter is relatively slight on IV curve. On the other hand on gm/Id (which is one of the key figures of merit in analog design), in figure 1.c & d, we observe clearly the improvement by using a new model of non-uniform DIT particularly evident on gm/ID curves.
The proposed model for SET has been implement in a Verilog-A code that is based on a finite number of RC circuits (cf figure 2.a). The input of the model are particle parameters, the ambipolar diffusivity and the splitting width. Finally, such a formalism makes the SET model suitable for SPICE circuit simulations and we showed some useful SPICE applications (cf figure 2.b).

Perspectives

For PSP we continue our effort to improve accuracy in accordance with industrial expectation. For SET, such a formalism makes the model suitable for SPICE simulations.

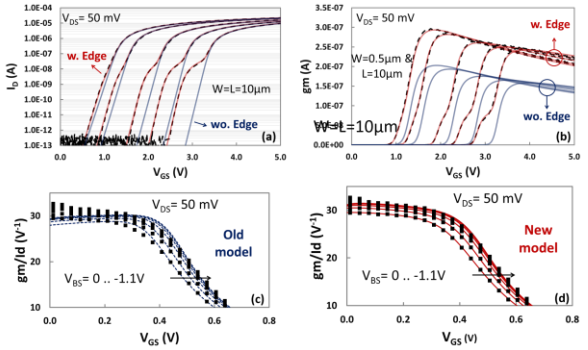


Figure 1: Comparison between experiments (dotted line) and model (red line with and blue line without new model) for linear current (I_D) (a), first derivative (gm) (b), gm/Id versus without (c) and with (d).

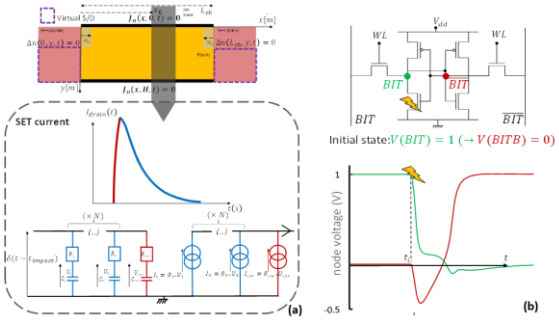


Figure 2: (a) Illustration of physical system with the SET current pulse with the equivalent circuit model proposed. (b) SPICE simulation of SEU occurrence in a SRAM cell using our model.

RELATED PUBLICATIONS:
[1] S. Martinie et al., SISPAD, 2018, DOI: 10.1109/SISPAD.2018.8551712
[2] N. Rostand et al., SISPAD, 2018, DOI: 10.1109/SISPAD.2018.8551633

Strain Maps And Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets FETs

RESEARCH TOPIC:

MOSFET, gate-all-around nanosheet, 5 nm node and beyond, replacement-metal-gate-process, SPICE, NSP model.

AUTHORS:

S. Barraud, S. Reboh, B. Previtali, V. Lapras, R. Coquand, J.-M. Hartmann, S. Martinie, N. Bernier (M-P. Samson, N. Loubet).

ABSTRACT:

A comprehensive study going from the integration of 3D stacked nanosheets Gate-All-Around (GAA) MOSFET devices to SPICE modeling is proposed. Devices are fabricated on SOI substrates using a replacement high-κ metal gate (RMG) process and self-aligned-contacts. Strain, stress, and mechanical relaxation in fin-patterned Si/SiGe multilayers are investigated. Back-biasing is also efficiently used to highlight a drastic improvement of electrostatics in the upper GAA Si channels. Advanced electrical characterization of these devices enabled us to calibrate a new version of physical compact model (NSP) in order to assess the performance of ring oscillators for different configurations of GAA FETs integrating up to 8 vertically stacked Si channels.

SCIENTIFIC COLLABORATIONS: STMicroelectronics (France), IBM research (USA).

Context and Challenges

After being proposed and developed a little more than ten years ago, stacked nanosheets (NS) gate-all-around (GAA) MOSFETs are becoming an industrial reality. After FinFET, GAA multi-channels are a new class of advanced CMOS delivering higher performances, consuming less and pushing further scaling limits. Research conducted over the last three years has allowed to make major advances to now place this novel technology in the roadmap of leading chipmakers.

Main Results

In this work, advanced transmission electron microscopy is used to investigate strain and stress relaxation effects in fin-shaped structures of (Si/SiGe) multilayers. With experimentally validated numerical models based on a finite element method (FEM), we provided quantitative descriptions of strain and stresses in the structures [1] as shown in fig. 1.

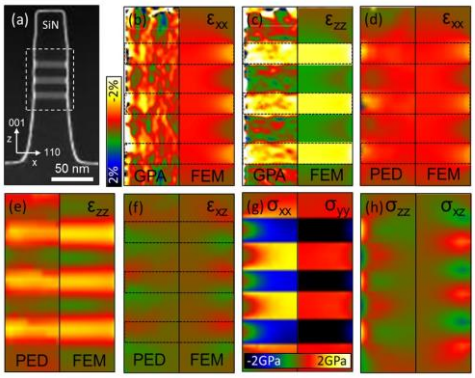


Figure 1: Cross-sectional dark-field STEM micrograph of Si/SiGe multilayers. Strain maps obtained by GPA for (b) ε_{xx} and (c) ε_{zz} and by PED for (d) ε_{xx}, and (e) ε_{zz}, and (f) ε_{zx}. Calculated strain (FEM) are shown in the right side of the Images.

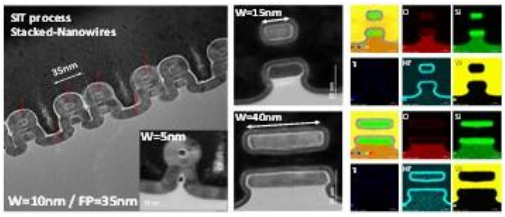


Figure 2: TEM images of (SiGe/Si) fins obtained by SIT which have a fin pitch of 35nm and a W=10nm width. A wide range of W is considered.

Then, GAA stacked-NS FETs (Fig. 2) are fabricated with a RMG process and self-aligned contacts. The impact of size (W, gate length) and substrate orientation on electrostatics and the overall performance of stacked wires n-FETs is studied. A good electrostatic control is shown despite lower trigate Si channel (DIBL=80mV/V at L_G=20nm). Next, back-biasing was used to tune the threshold voltage of the lower trigate Si channel and focus on the electrostatics properties and transport in the upper GAA Si channel. Effectiveness of reverse back-biasing channel modulation resulted in a drastic improvement of electrostatic properties in GAA structures. This can be considered as an additional lever to offer more power/perf. flexibility in 3D stacked channels. Finally, NSP compact model has been validated with experimental data on large ranges of applied biases and device geometries. The good agreement with experiment demonstrated the accuracy of our physical compact model to predict GAA stacked-NS operation. Then, based on this model, SPICE modeling allowed the assessment of ring oscillator performance for different configurations of GAA FETs integrating up to 8 vertically stacked Si channels [2].

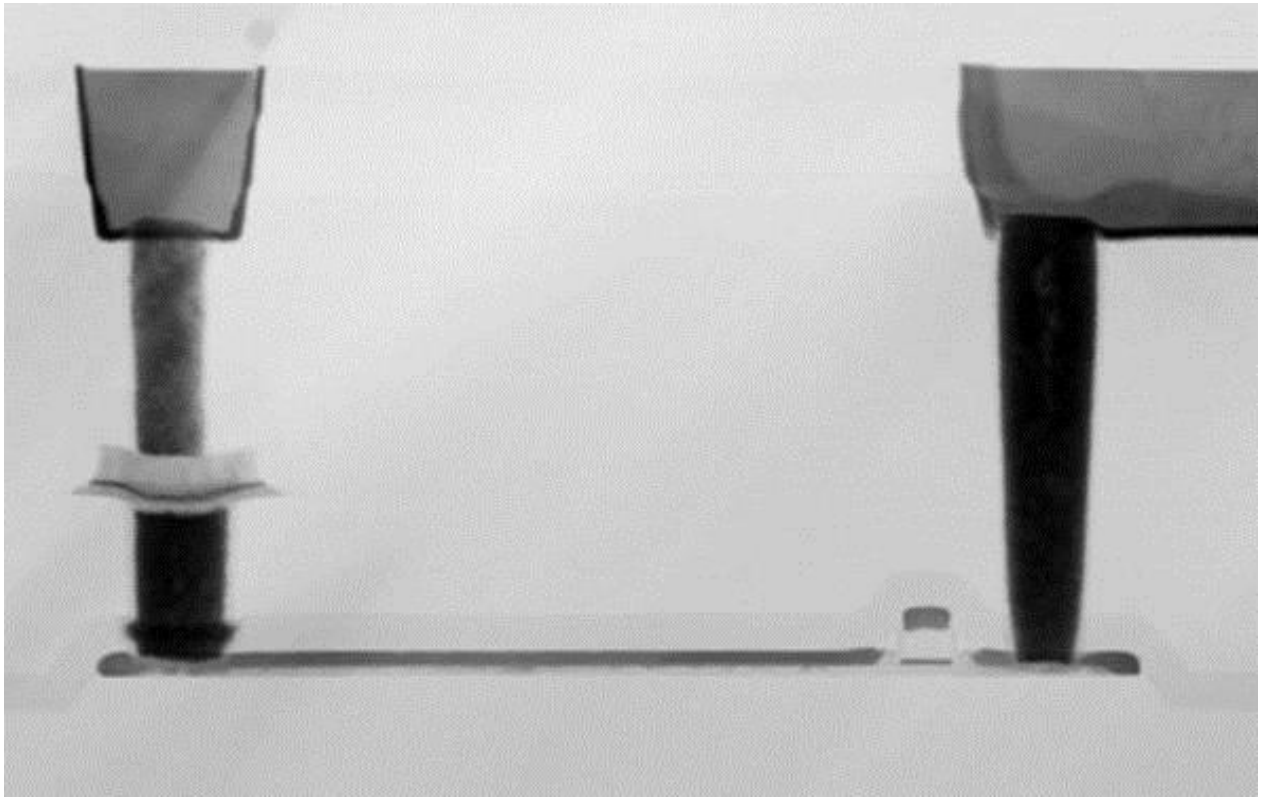
Perspectives

Further developments to increase the drive current per layout footprint and the predictability of compact modeling for stacked-nanosheet devices are in progress.

RELATED PUBLICATIONS:

[1] S. Reboh et al., Appl. Phys. Lett. 112, 051901 (2018); DOI: 10.1063/1.5010997

[2] S. Barraud et al., in IEDM Technical Digest, pp. 21.3.1-21.3.4 (2018); DOI: 10.1109/IEDM.2018.8614507



O2 MEMORIES

- **OTS Selectors for Emerging Memories**
- **Resistive Memories for Spiking Neuromorphic Circuits**
- **Next Generation of Phase-Change Memory: Performances Challenges Enabled by Scientific and Technology Innovation**
- **RRAM Reliability Improvement**

OTS Selectors for Emerging Memories

RESEARCH TOPIC:

Backend Selector, Ovonic Threshold Switching (OTS)

AUTHORS:

A. Verdy, M. Bernard, G. Bourgeois, P. Noé, J. Garrione, M. C. Cyrille
G. Navarro and E. Nowak

ABSTRACT:

Back-End selector technology is fundamental for the implementation of high-density 3D Resistive Crossbar Arrays. Among the several Back-End selector devices developed in the last years, Ovonic Threshold Switching selector (OTS) represents a promising candidate. The development of OTS devices requires material as well as device engineering. At LETI, both these activities are ongoing in order to achieve highly reliable and BEOL-compatible selector devices. Our investigations highlight the OTS and the memory parameters that can influence the functionality of a crossbar array, in particular during the reading operations. High temperature reliability, high endurance and low leakage current achieved in our OTS devices represent key achievements towards reliable and high-density crossbar based architectures.

SCIENTIFIC COLLABORATIONS: STMicroelectronics

Context and Challenges

Resistive Crossbar Array (RCA) represents the most suitable technological solution as Storage Class Memory (SCM) to overcome the actual memory architecture bottleneck represented by the huge latency difference between the main memory (DRAM) and the storage (Flash Memory). Moreover, it opens the way for new paradigms for non-Von Neumann architectures such as neuromorphic accelerators or in-memory computing. RCA requires the integration in the Back-End-of-Line (BEOL) of the fabrication, making essential for its functionality a BEOL access selector device, such as the Ovonic Threshold Switching selector (OTS). The OTS engineering and reliability becomes fundamental to achieve high RCA performances.

Main Results

In order to push the OTS selector performances, we analyzed the interaction of the material with the surrounding electrodes. We highlighted the important diffusion of the metallic electrode inside the OTS material that occurs during the operations of the device, resulting in an important increased and dispersed leakage current. Inserting a thin carbon layer as diffusion barrier results in an ultra-low leakage current and improved reliability (Fig.1).

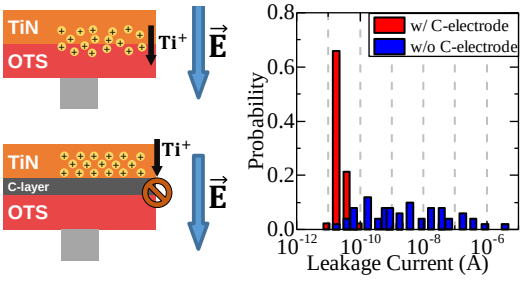


Figure 1: Carbon layer is used as diffusion barrier, enabling ultra-low leakage current and improved reliability of the devices.

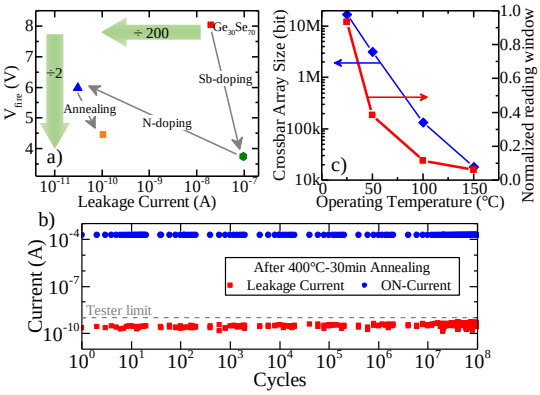


Figure 2: Material engineering in Ge-Se-Sb-N system permits to achieve devices featuring low leakage current, low operating voltage (a), BEOL thermal budget compatibility and high endurance (b). Simulations of the reading window and of the array size as a function of the operating temperature for an RCA integrating our optimized OTS selector (c).

We show that in the Ge-Se-Sb-N system, low operating voltage, low leakage current, BEOL compatibility and high endurance (Fig. 2a, b) are achieved thanks to proper doping and a specific thermal annealing procedure responsible for a beneficial material reorganization.

Investigations on the read operation highlighted the need for reliable measurements of new metrics, such as the OTS threshold current, and for the evaluation of the influence of the operating temperature on the OTS and on the memory parameters. We clearly showed how the final performance of the RCA depends on such parameters (Fig. 2c).

Perspectives

This work paves the way for further developments, targeting large crossbar arrays for SCM and neuromorphic applications. It enables design rules in order to optimize the OTS selector to fulfill the specifications required for the co-integration with different resistive memories (such as PCRAM, OxRAM or CBRAM).

RELATED PUBLICATIONS:

[1] A. Verdy et al., IEEE International Electron Devices Meeting (IEDM), 2018, San Francisco, CA, USA, DOI: 10.1109/IEDM.2018.8614686
[2] A. Verdy et al., 2018 IEEE International Memory Workshop (IMW), Kyoto, Japan, DOI: 10.1109/IMW.2018.8388834
[3] A. Verdy et al., 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, DOI: 10.1109/IRPS.2018.8353635

Resistive Memories for Spiking Neuromorphic Circuits

RESEARCH TOPIC:
RRAM, TCAM, neuromorphic circuits, characterization, reliability, performance, artificial synapses

AUTHORS:
E. Vianello, D. R. B. Ly, J.-P. Noel, B. Giraud, A. Grossi, A. Valentian, E. Nowak (D. Querlioz), (G. Indiveri)

ABSTRACT:
Resistive Memory (RRAM) technology can play a crucial role for the design of neuromorphic circuits. First, RRAMs can be used to reproduce artificial synapses. We demonstrated that a neural network that learns through the Spike Time Dependent Plasticity algorithm (an on-line and unsupervised algorithm) not only holds up well against RRAM non-ideality, but they can draw benefits from it. Second, RRAMs can play a crucial role in the design of asynchronous routing for implementing scalable multi-core neuromorphic architectures. We demonstrated that RRAM-based ternary-content addressable memory (TCAM) circuits meet the performance and reliability requirements of multicore neuromorphic processors.

SCIENTIFIC COLLABORATIONS: Univ. Paris-Sud, University of Zurich and ETH Zurich

Context and Challenges
Resistive switching memories (RRAMs) represent a promising technology for building neuromorphic circuits. First, they have attracted wide interest as adaptive synaptic elements in artificial bio-inspired Spiking Neural Networks (SNNs). Second, we have recently proposed RRAM-based ternary-content addressable memory (TCAM) circuits for the design of asynchronous routing in multicore neuromorphic processors

Main Results
First, we investigated the role of RRAM non-idealities (resistance variability, number of resistance levels) in Spiking Neural Networks (SNNs) based on RRAM synapses. We analyzed the role of synaptic (RRAM) non-idealities during on-line unsupervised learning by Spike-Timing Dependent Plasticity (STDP) for detection in dynamic input data and classification of static input data. We demonstrated that SNNs are not only robust to synaptic variability, but can also draw benefit from it. RRAM variability can be beneficial as it increases the range of synaptic weight values available during learning. For detection applications, binary RRAM technology is well-suited to implement synaptic elements as only one RRAM device per synapse is needed. On the other hand, for classification applications, multilevel conductance synapses are necessary to achieve the best performance; a synaptic compound composed of at least 10 OxRAMs per synapse is required.
Second, we fabricated and fully characterized a RRAM-based ternary-content addressable memory (TCAM) circuit. TCAM circuits allow searching for stored information by its content, as opposed to classic memory systems in which a memory cell's stored information is retrieved by its physical address. They shorten the search time compared to classic memory-based search algorithms, as all the stored information is compared with the searched data in parallel, within a single clock cycle. However, conventional SRAM-based TCAM circuits are usually implemented with 16 CMOS transistors, which limits storage capacity of TCAMs to tens of Mbs in standard memory structures, and takes up valuable silicon real estate in neuromorphic computing spiking neural-network chips. The fabricated RRAM-based TCAM circuit replaced SRAM cells with RRAM to reduce the number of required transistors to two (2T), and to two RRAMs (2R), which is the most compact structure for these circuits produced to date. In addition, the RRAMs were fabricated on top of the transistors, which also consumed less area. This suggests such a 2T2R structure can decrease the required TCAM area by a factor of eight compared to the conventional 16-transistor TCAM structure. However, while using RRAMs in TCAM circuits significantly reduces both silicon chip area needed and power consumption, this approach brings new challenges: first, the size of the TCAM memory is limited by the ratio between the ON and OFF states of the RRAM cells (~10-100). Second, RRAMs have a limited endurance with respect to CMOS transistors, which can affect the lifespan of the system. The TCAM cells used in multicore neuromorphic processors are typically small in size and are programmed only at network configuration time, thus they perfectly meet the performance and reliability of the proposed circuit.

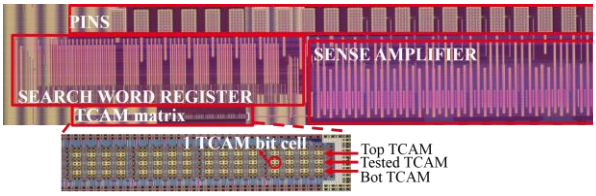


Fig. 1 Fabricated and tested RRAM-based TCAM circuit.

Perspectives
These results give some guidelines to design SNNs based on RRAM to implement both synapses and routing.

RELATED PUBLICATIONS:
[1] D.R.B. Ly et al., IEEE International Electron Devices Meeting (IEDM), 2018, San Francisco, CA, USA, **DOI:** 10.1109/IEDM.2018.8614603
[2] D.R.B. Ly et al., J. Phys. D: Appl. Phys. 51, 2018, https://iopscience.iop.org/article/10.1088/1361-6463/aad954/meta
[3] A. Grossi et al., ,IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol. 26, NO. 12, Dec. 2018,: 10.1109/TVLSI.2018.2805470

Next Generation of Phase-Change Memory: Performances Challenges Enabled by Scientific and Technology Innovation

RESEARCH TOPIC:

Non-volatile Resistive Memory, Phase-Change Memory (PCM), chalcogenides, Storage Class Memory (SCM)

AUTHORS:

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ABSTRACT:

We propose different ways of engineering the Phase-Change Memory device targeting a highly energy efficient cell. We show that electrical and thermal confinement improvement of the phase-change material enables a high reduction of the programming current, achieved also by the optimization of the device architecture, in particular in the case of a confined structure. Furthermore, we demonstrate the reduction of thermal losses by the tuning of the thermal conductivity of the dielectrics surrounding the phase-change material. Finally, we propose some considerations about material engineering, as demonstrated in SLL-PCM (superlattice like PCM) whose thermal properties could lead to significantly improved efficiency of the cell.

SCIENTIFIC COLLABORATIONS: CNRS-LTM, STMicroelectronics

Context and Challenges

Phase-Change Memory (PCM) is today the most mature among innovative back-end non-volatile memory technologies (NVM). Its recent commercialization to address stand-alone Storage Class Memory (SCM) applications demonstrates its advanced state in terms of industrialization. Moreover, PCM technology is versatile enough to meet different applications' requirements and recent progress in material engineering opens new ways to target both data retention and programming speed. Thus, charge based Flash memory will be highly challenged by PCM at the low power portable applications age, making the cell efficiency a must for next generation of NVM.

Main Results

The PCM « confined structure » allows a six-fold reduction of the current density with respect to a heater based structure, thanks to a drastic material volume and thermal confinement. This cell structure optimization forces the localization of the amorphous region along the sidewall of the structure, creating an active region fully amorphized at once which explains the abrupt transition between the SET and the RESET state (Fig. 1).

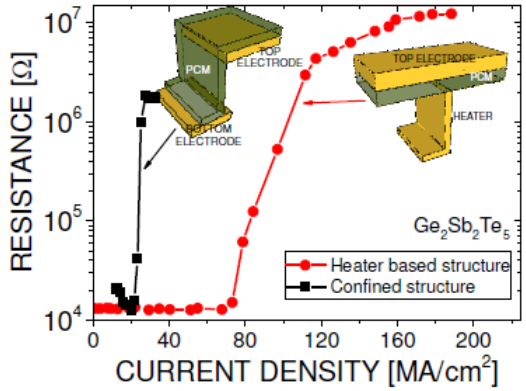


Figure 1: Programming characteristics for a standard PCM device (heater based) and an optimized Confined structure.

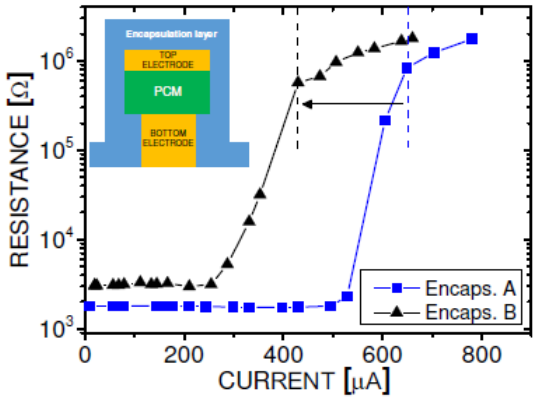


Figure 2: Programming characteristics of two PCM devices integrating two different encapsulation layers.

A further reduction of the programming power can be achieved thanks to the engineering of the dielectrics that surround the device. The lower thermal conductivity of layer B with respect to layer A, preventing heat losses, allows a RESET operation at lower current (~ 30% of reduction) (Fig. 2). We also investigated a standard PCM lance-type cell integrating an optimized GeS_2/Sb_2Te_3 material obtained by co-sputtering, leading to both an electrical (i.e lower volume) and a thermal confinement improvement (i.e a higher power efficiency). Indeed, Sb_2Te_3 nanocrystals formation in GeS_2 amorphous matrix, so called GSST based PCM cell, leads to a great reduction of the programming current (more than ten times) compared to standard $Ge_2Sb_2Te_5$.

Perspectives

Beyond PCM device engineering, new thermal properties can be involved in multilayers phase-change films, in particular phonon scattering at interfaces creating a huge thermal confinement along the z-axis of the cell. These developments reveal the possibility to engineer and target high-energy efficient next generation PCM, for low power/high density memory applications.

RELATED PUBLICATIONS:

[1] G. Navarro et al., IEEE International Memory Workshop (IMW), 2018, Kyoto, Japan, DOI: 10.1109/IMW.2018.8388845

[2] G. Bourgeois et al,,Non-Volatile Memory Technology Symposium (NVMTS), 2018, Sendai, Japan ,http://www.cies.tohoku.ac.jp/nvmts2018/program/day_2.html

RRAM Reliability Improvement

RESEARCH TOPIC:
Resistive Memory, Non Volatile Memory, reliability

AUTHORS:
G. Sassine, D. Alfaro Robayo, J.-F. Nodin, J. Coignus, C. Cagli, E. Nowak, G. Molas, (Q. Rafhay, G. Ghibaudo)

ABSTRACT:
We deeply investigated RRAM endurance at the statistical level. Understanding of RRAM endurance fail is analyzed experimentally on 4 kb memory arrays and theoretically thanks to numerical simulations. Then, reliability improvement is achieved by optimizing programming energy on RRAM 1T1R kb arrays. SET and RESET programming patterns are optimized with programming current of 50 µA, to minimize the energy provided to the system, maintaining sufficient widow margin on resistance distribution tails. Maximum endurance was improved of about 2 cycling decades up to 10^7 cycles, error tails were significantly reduced even for programming currents of 50 µA, required for low power applications.

SCIENTIFIC COLLABORATIONS: IMEP LAHC CNRS (Grenoble, France)

Context and Challenges
RRAM variability is today the main roadblock to be solved before mass production could be envisaged. In this context, reliability improvement has to be addressed by analysis at the statistical level, studying RRAM arrays. In this work, we analyze RRAM endurance failure at the statistical level and propose a model to perform predictive extrapolations [1]. We optimize SET RESET patterns by adjusting programming energy, resulting in significant endurance and retention improvement [2]. Finally, we significantly reduce RRAM programming consumption of slow tails in memory populations [3].

Main Results
Results were obtained on RRAM technologies integrated in our 200 mm test vehicle. Both HfO_2/Ti OXRAM and Al_2O_3/$CuTe_x$ CBRAM were investigated.
We demonstrated that RRAM maximum number of cycles (endurance) follows a log normal distribution law (Fig.1). Endurance dispersion depends on RRAM stack (materials and thicknesses). Adjusting RESET voltage allows to optimize endurance statistics and reduces cycling performances dispersion.

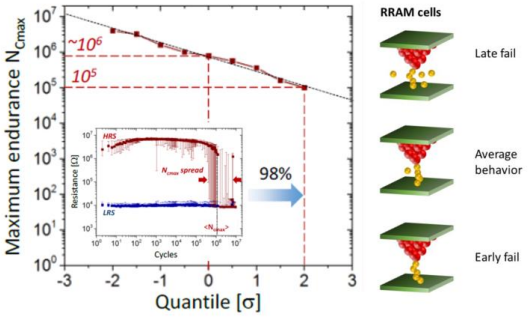


Figure 1: RRAM (Al_2O_3/$CuTe_x$) maximum endurance distribution measured on 4kb arrays.

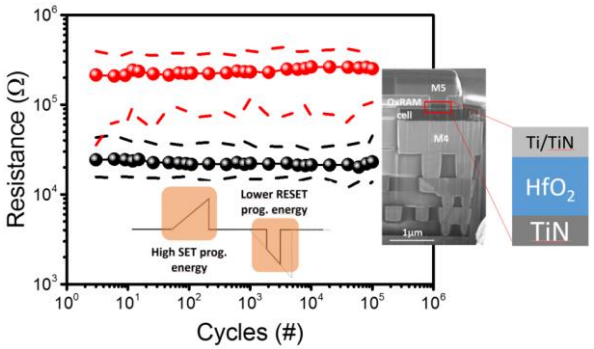
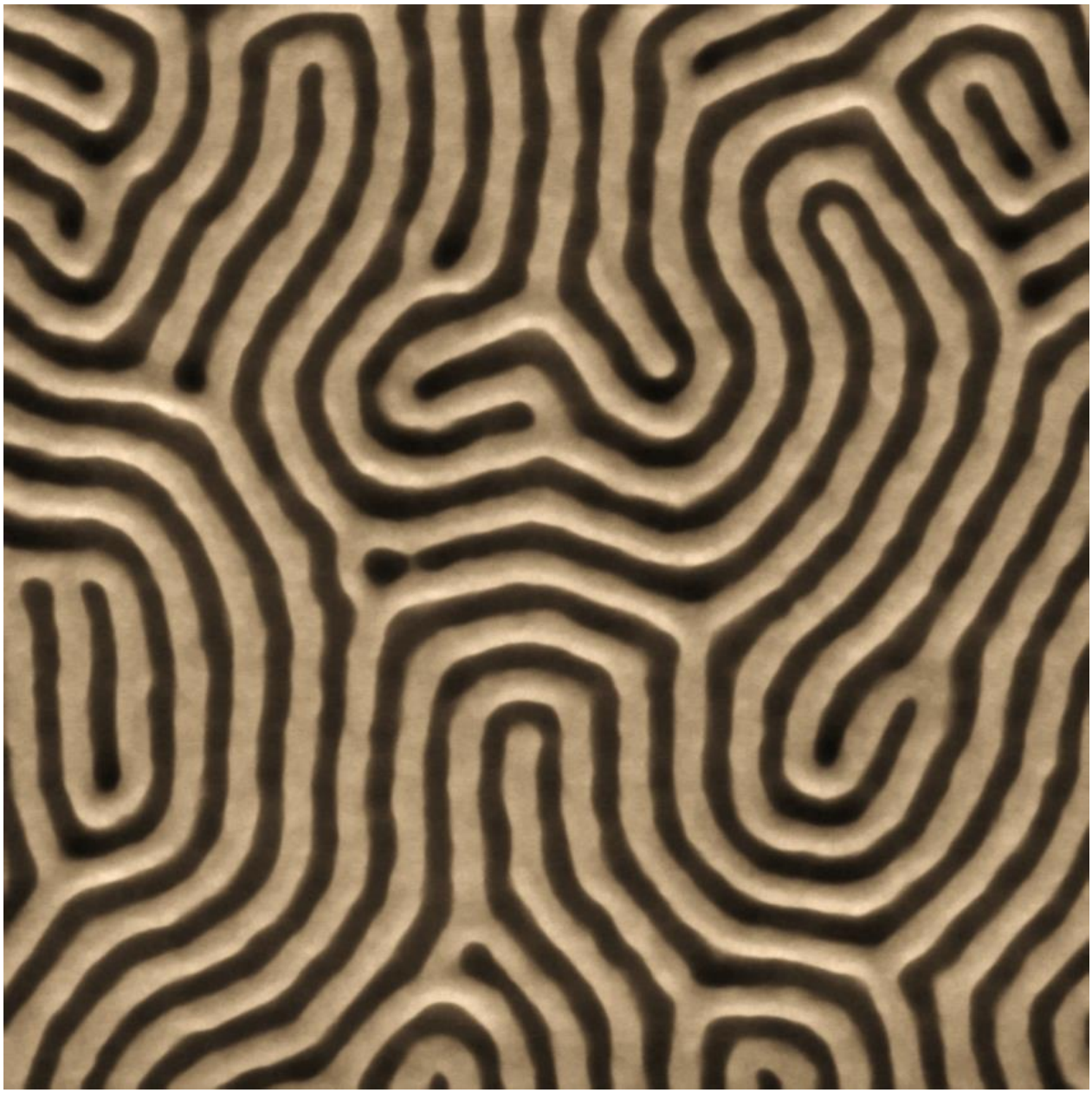


Figure 2: OxRAM endurance on 4 kb arrays with optimized patterns showing no overlap of ON (black) and OFF (red) resistances (dashed lines: 95% of the cells).

RRAM endurance evaluation at the array level is therefore mandatory to confront RRAM device reliability with industrial requirements before technology ramp up could be envisaged.
Then we improve RRAM endurance by optimizing programming energy on HfO_2/Ti OXRAM kb arrays. Optimized ramp voltage based programming scheme minimizes the energy provided to the system RESET. It allows to improve maximum endurance by about 2 decades, to insure stable median window margin at 10^7 cycles and to maintain window margin at 2σ after 10^6 cycles at 50 µA for low power applications.

Perspectives
Significant improvement of RRAM reliability (endurance, retention, consumption) was proposed, optimizing programming scheme, thanks to the understanding of the device at the microscopic level. Next step will consist in the co-integration of a back-end OTS selector with the memory and analysis of impact of RRAM variability on the device performances.

RELATED PUBLICATIONS:
[1] D. Alfaro Robayo et al., 2018 Int. Symp. on VLSI Tech., Systems and Application (VLSI-TSA), Hsinchu, Taiwan, DOI: 10.1109/VLSI-TSA.2018.8403856
[2] G. Sassine et al., 2018 IEEE International Memory Workshop (IMW), Kyoto, Japan, DOI: 10.1109/IMW.2018.8388843
[3] G. Sassine et al., IEEE Journal.of the Electron Device Society, 6, (2018), DOI: 10.1109/JEDS.2018.2830999



O3 PATTERNING

- **Innovative Etching Approach for Low-k Spacer Patterning**
- **Fine-Tuning of Surface Energies for DSA Patterning**
- **Pushing Line Roughness Metrology Techniques to their Limits**
- **Lithography Computational Aspects for Mask Writing**
- **Advanced Design Correction for Wafer Scale NanoImprint Process**
- **Multibeam Lithography : Process Integration Flow and Associated Metrology**

Innovative Etching Approach for Low-k Spacer Patterning

RESEARCH TOPIC:
Thin layer etching, Low-k, spacer fabrication, SiCO, FDSOI

AUTHORS:
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ABSTRACT:
Low-k spacer etching realization is considered today as one of the most challenging processes for the manufacturing of fully depleted silicon on insulator devices. Indeed, such films, required to replace conventional silicon nitride to improve device performances, leads to critical patterning issues due to its high sensitivity to fluorocarbon based plasma. To overcome these issues and meet the stringent etch requirements of traditional spacer realization (no foot formation, critical dimension control below one nanometer), a new process was developed to etch SiCO Low-k spacer.

SCIENTIFIC COLLABORATIONS: STMicroelectronics

Context and Challenges
Spacer etching is still challenging for the production of high performance Fully Depleted Silicon On Insulator (FDSOI) device production. A trade-off has to be found between silicon germanium (or silicon) recess, foot formation and spacer faceting on top of the hard mask directly impacting the device performances. This challenge is all the more critical for the introduction of low-k film instead of traditional silicon nitride. Indeed, such low-k films are more sensitive to fluorocarbon-based chemistries, leading to critical patterning issues. To overcome these issues, we proposed a new etch approach for silicon oxycarbide (SiCO) [1] concerns. The new etching process is based on two steps. The film is firstly modified by a H_2 plasma (labeled as SiCO*) performed in an Inductively-Coupled (ICP) Plasma chamber followed in a second step by a 1% HF wet cleaning to remove the modified layer selectively to the non-modified materials (SiCO, Si or SiGe).

Main Results
A precise control of the SiCO* film damage thickness, can be tuned using the plasma operating conditions such as bias voltage or process time (Fig.1).

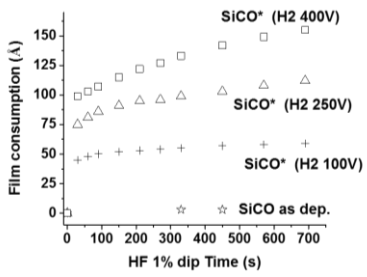

Figure 1: Evolution of the SiCO* film consumption as a function of bias voltage and HF dip time.

Infrared spectroscopy analyses revealed that the H_2 plasma exposure leads to SiCO film oxidation with important Si-H and silanol group formation. This carbon depletion confirmed by XPS after H_2 plasma (converting the SiCO film into SiOxHy film) is responsible at the first order for the higher etch rate when SiCO* is dipped in liquid phase HF.
Application on patterns showed that this approach offers an interesting alternative to conventional fluorocarbon based chemistries. Indeed, after H_2 plasma followed HF dip, the SiCO spacer can be etched without underneath film modification, no foot formation and less than 2 nm lateral consumption (Fig.2).

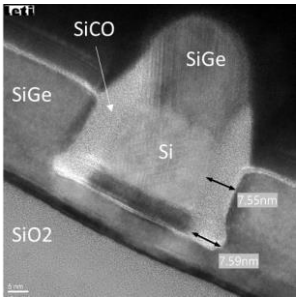

Fig 2: TEM image of a 14 nm FDSOI transistor gate. SiCO spacer etching was performed by H_2 plasma implantation followed by 1% HF dip followed by SiGe epitaxial growth.

A consumption of the SiO_2 hard mask (not compatible with long HF dip time) is also observed in Fig. 2, explaining the EPI regrowth on top of the gate. Therefore, a tradeoff between the bias voltage and the HF dip time is required. Otherwise, the replacement of the hard mask by a film less sensitive to the HF dip would be a promising solution.

Perspectives
The interest of low-k SiCO spacer etching using a combination of H_2 plasma and HF dip has been demonstrated. In an upcoming study, we will optimize the developed processes and extend to other low-k films.

RELATED PUBLICATIONS:
[1] N.Posseme et al, JVST B, 2018, https://doi.org/10.1116/1.5038617

Fine-Tuning of Surface Energies for DSA Patterning

RESEARCH TOPIC:
Advanced patterning, directed self-assembly, block copolymers

AUTHORS:
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ABSTRACT:
Directed self-assembly (DSA) of block copolymers (BCP) is a promising solution for advanced patterning of sub-10 nm technology nodes. Known for high-resolution capabilities, low-cost and ease process integration, DSA continues to attract the semiconductor industry. DSA technology is suitable for various patterning as line and space, contact shrink and multiplication and pillars. Recently, CEA-Leti has developed original DSA approaches from lab scale to industrial scale using its DSA pilot line and advanced BCP materials. The fine-tuning of surface energies and optimization of key lithographic parameters are reported.

SCIENTIFIC COLLABORATIONS: Arkema, Brewer Science, SCREEN, AMAT, LTM, LCPO, STMicroelectronics

Context and Challenges
Affordable, simple, versatile: DSA is still highly investigated as a sub-10 nm feature lithography technique to implement in the CMOS industry. DSA is used to target different lithography applications: creation of gratings of line and space, contact hole shrink and multiplication, and pillar patterning.

Firstly, in order to properly align the BCP, guide templates are created by conventional optical lithography. The surface energy of these guiding patterns, with respect to both monomers, needs to be finely tuned. Secondly, process parameters such as critical dimension uniformity (CDU), overlay and line roughness require to be optimized to meet stringent specifications.

Main Results
Independent control of surface energy between the bottom and the sidewalls of a topographical guiding structure is critical for DSA process optimization.

For a contact hole shrink process, an embedded layer with tunable surface properties for DSA graphoepitaxy was evaluated and optimized [1]. A thin protective layer was placed between the hard mask guiding template and the embedded layer. This new layer allows to preserve the surface properties of the embedded layer during guiding template etching, resulting in better control of the polymer residual thickness (a few nanometers) and uniformity (< 1 nm) at the bottom of the guiding template. In turn, it will facilitate the subsequent DSA pattern transfer.

For a line/space graphoepitaxy DSA process, an innovative UV-assisted method was developed for precise control of the surface energy of topographic grating [2]. Wafer-scale exposure of polystyrene (PS) lines using 193 nm wavelength radiation enables to reduce significantly the line roughness as illustrated in the Figure 1.

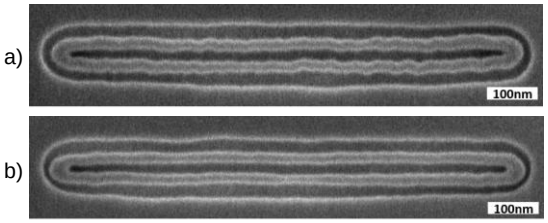

Figure 1: Top-view SEM images of PS lines transferred into 12nm-thin single crystalline silicon (a) without any PS treatment, (b) with a PS treatment before etching.

Advanced CD-SEM metrology utilizing the back-scattered electron imaging (BSE) mode [3] allowed to detect unwanted thin and buried polymer residues and subsequently to optimize the process (Fig. 2). This process has been integrated in a manufacturing flow of 22 nm lateral nanowire transistors, leading to an electrical demonstrator.

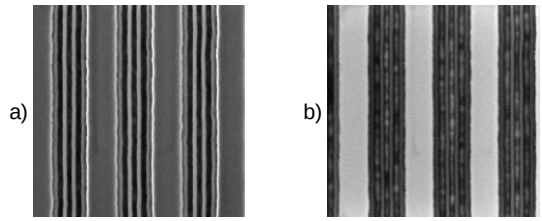

Figure 2: Top-view SEM images of line/space graphoepitaxy (a) with SE mode, (b) with BSE mode (brightness between lines indicates minimization of polymer residues).

Perspectives
The DSA team will focus on a novel approach to align the BCP by chemo-epitaxy and create the guides by sidewall image transfer (SIT). Line/space patterns with CDs of 15 nm down to 7 nm will be patterned. Control of surface energies and line roughness reduction are key elements to succeed.

RELATED PUBLICATIONS:
[1] F. Delachat et al., Nanoscale, 10 (23), 2018, http://dx.doi.org/10.1039/c8nr00123e
[2] P. Pimenta-Barros et al., in Proc. SPIE, 10584, 2018, http://dx.doi.org/10.1117/12.2297407
[3] R. Le Tiec et al., in Proc. SPIE, 10586, 2018, https://doi.org/10.1117/12.2299634

Pushing Line Roughness Metrology Techniques to their Limits

RESEARCH TOPIC:
Line roughness, characterization, lithography

AUTHORS:
J. Reche, (M. Besacier), P. Gergaud, Y. Blancquaert

ABSTRACT:
The need for roughness metrology is recognized in the International Technology Roadmap for Semiconductors (ITRS). In order to reduce the edge or width roughness of lines, a metrology method is needed to quantify it. Firstly, roughness standard samples were manufactured and used as standards to evaluate the performances of several metrology tools. The capability of each of these roughness measurement techniques was evaluated in terms of resolution, access to frequency information, acquisition and treatment throughput, and maturity.

SCIENTIFIC COLLABORATIONS: CNRS/LTM

Context and Challenges

The control of line roughness presents a huge challenge for the lithography step in the semiconductor industry. For advanced nodes, this morphological aspect reaches the same order of magnitude than the Critical Dimension (CD), which leads to an increased power consumption by transistors and devices. For the 7 nm node, the acceptable roughness is only 0.7 nm, which means that the resolution of the measurement has to be at the angstrom scale. Hence, an adapted metrology is required for the control of roughness. The current technique for CD analysis and roughness extraction is the Critical Dimension Scanning Electron Microscopy (CD-SEM), but many other metrology techniques as Atomic Force Microscopy, Small-Angle X-ray Scattering (SAXS) and Optical Scatterometry (OCD) are also developed.

Main Results

First of all, roughness standard samples were manufactured [1]. The preliminary steps were to demonstrate the patterning methodology and the line roughness metrology, using periodical roughness samples.

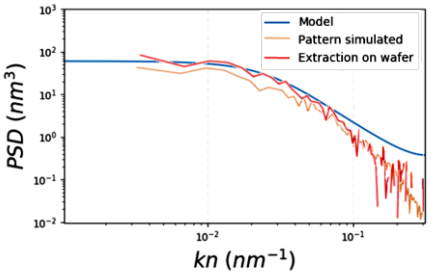

Figure 1: Example of programming roughness with PSD plots obtained through: model calculation, simulation of SEM images and experimental measurements

Further, programming of roughness based on Power Spectral Density (PSD) with Auto-Correlation Function (ACF) model was used to achieve roughness close to a real roughness case (Fig.1). The samples have been written using e-beam lithography taking into account the specific constraints of the different metrology techniques.

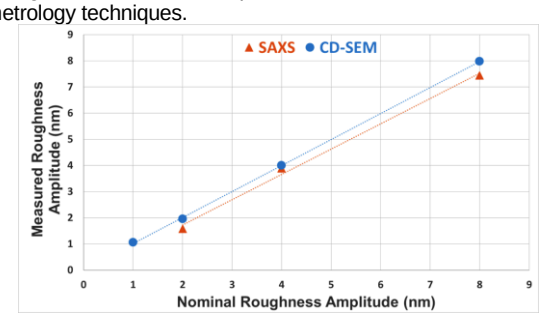

Figure 2: Extracted roughness amplitude with CD-SEM and SAXS compared at nominal roughness amplitude

These specific lines gratings programmed samples were characterized with three different methodologies [2], CD-SEM, OCD and SAXS and compare in terms of roughness resolution, access to frequency information, acquisition and treatment throughput and maturity. This comparison highlights that (i) OCD can detect roughness but needs calibration, (ii) CD-SEM and CD-SAXS give similar results (Fig. 2), close to the nominal roughness values designed.

Perspectives

The next step for sample manufacturing is to integrate within the design the natural line roughness in order to avoid reference subtraction and so to obtain real standard samples. We are also working on data fusion of the different techniques CD-SEM/CD-SAXS/OCD. The development of a line roughness hybrid metrology using neural network is in progress that will exploit the strengths of each methodology.

RELATED PUBLICATIONS:
[1] J. Reche et al., 34th European Mask and Lithography Conference, 2018, http://dx.doi.org/10.1117/12.2327095
[2] J. Reche et al., Journal of Micro/Nanolithography, MEMS, and MOEMS 17 (4), 2018, http://dx.doi.org/10.1117/1.JMM.17.4.041005

Lithography Computational Aspects for Mask Writing

RESEARCH TOPIC:

Computational lithography, mask data preparation, proximity correction, computational metrology

AUTHORS:

L. Audebert, S. Bérard-Bergery, (J. Bustos), A. Fay, A. Forier, J. Hazart, J.B. Henry, A. Girodon, E. Guyez, L. Perraud, J. Pradelles, P. Quéméré.

ABSTRACT:

Optical lithography for advanced nodes uses complex Optical Proximity Corrections (OPC) resulting in sub-100 nm curvilinear mask patterns. A dedicated small-shots correction was developed to substantially improve the fidelity of demanding aggressive mask patterns written directly with Variable Shaped Beam (VSB) e-beam technology. Additionally, in-line 3D metrology is of key importance to further improve and control the lithography processes. We demonstrate that model-based Scanning Electron Microscope (SEM) 3D non-destructive metrology is a promising in-line technology to reconstruct 3D topography with a rather high precision despite the typical SEM noise level.

SCIENTIFIC COLLABORATIONS: ASELTA Nanographics, Université Grenoble Alpes LJK

Context and Challenges

Inverse Lithography Technology (ILT) and advanced photonics patterns push e-beam VSB mask writing technology to its limits. Beyond 50 nm resolution, small VSB shots are not well controlled due to machine imperfections inducing mask patterns errors. A specific mask data preparation (MDP) solution is proposed to overcome these errors. On the other hand, lithography process optimization for 3D complex architectures is demanding of accurate in-line 3D metrology. The ultimate accuracy of the reconstructed 3D geometry by model-based SEM 3D metrology is reported.

Main Results

New small-shots correction for Mask Data Preparation

VSB e-beam lithography technology exhibits pattern fidelity deviations and resolution limitations for small shots, typically below 50 nm. A small-shots model based on a geometry shot deformation law understands these limitations. This model was calibrated by measuring lines of different fracturing. We experimentally demonstrate a 10-fold decrease of Edge Placement Errors (EPE) on photonics and ILT patterns by using a dedicated small-shots correction (Fig. 1).

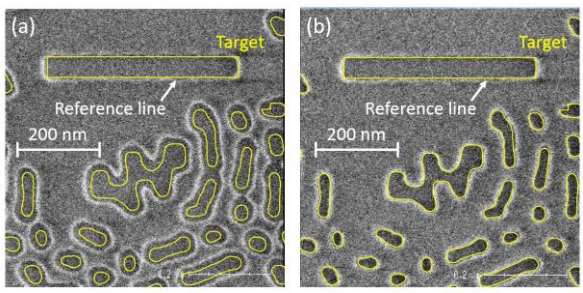

Figure 1: SEM images of ILT patterns printed on VSB e-beam tool (a) without and (b) with small-shots corrections.

3D SEM metrology accuracy

Assuming a perfect SEM model (Fig. 2) and considering a SEM noise level of 10%, sub-20 nm CD lines can be measured from top-view CD-SEM images with a precision of less than 1 nm. The height and the sidewall angle (SWA) dimensions can also be extracted from tilted SEM images, with acceptable uncertainties of 0.75 nm and 0.25°, respectively. Thus, model-based SEM metrology is a promising technology to reconstruct the 3D topography with a high level of confidence.

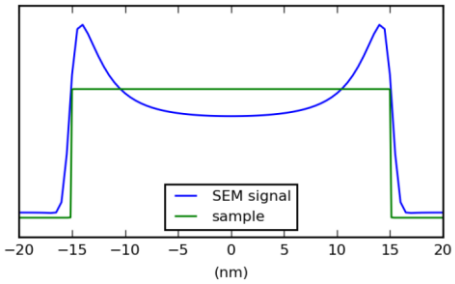

Figure 2: Simulated SEM image cut of a 30 nm wide line pattern.

Perspectives

The new small-shots correction can be used in production to improve the resolution and fidelity of VSB mask writers.
Innovations in model-based 3D SEM metrology will be pushed forward to make emerge in-line robust and accurate 3D SEM metrology technology to help in improving and controlling the lithography processes.

RELATED PUBLICATIONS:

[1] A. Fay et al., Proc. SPIE, 2018, http://dx.doi.org/10.1117/12.2501823
[2] J. Belissard et al., Proc. SPIE, 2018, http://dx.doi.org/10.1117/12.2323696

Advanced Design Correction for Wafer Scale NanoImprint Process

RESEARCH TOPIC:
Nanoimprint, proximity correction, distortion, metrology, design rules, bias modelling

AUTHORS:
H. Teyssèdre, P. Quéméré, (F. Delachat), F. Boudaa

ABSTRACT:
Nanoimprint lithography (NIL) technique sticks out from other conventional lithography processes by the fundamental mechanism involved to create the structures: it is no longer chemistry-based but related to resist flow within master cavities. Thanks to this technique, single step for 3D patterning and beyond CMOS applications becomes promising for features down to 50 nm. As the technology maturity starts to fit industry needs, CEA-Leti investigates the dimensional bias induced by the EVG process and developed the associated modelling based on pitch, orientation and position on the wafer.

SCIENTIFIC COLLABORATIONS: EV Group, Arkema

Context and Challenges
Since the recent developments of the nanoimprint lithography technology, this low cost patterning solution was introduced into high volume manufacturing [1], with two mains approaches: the full wafer imprint and the step and flash imprint. The key challenges to overcome are the master manufacturing (resolution and cost), the imprint materials (e.g. etching or optical properties) and the equipment capabilities. CEA-Leti focuses in 2018 on the process impact on the dimensional bias and the associated models. For these purposes, advanced calibration masters, dedicated metrology and innovative models have been investigated.

Main Results
The bias induced by the EVG process (SmartNIL™) raises from the shrink of the UV curable materials and the deformation of the soft stamp. These phenomena cause up to 12 % in our evaluation and needs advanced metrology capabilities to be captured (Fig. 1).

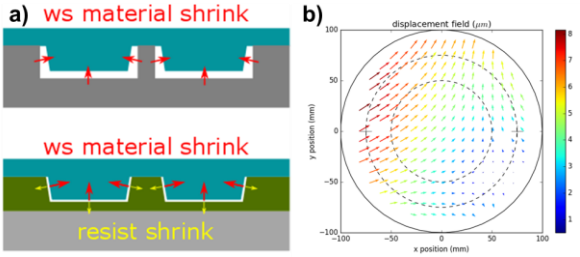

Figure 1: (a) Illustration of the shrink effect on the feature sizes during the soft stamp manufacturing and resist imprint, (b) Typical deformation map of the smartNIL™ process on a 200 mm wafer size.

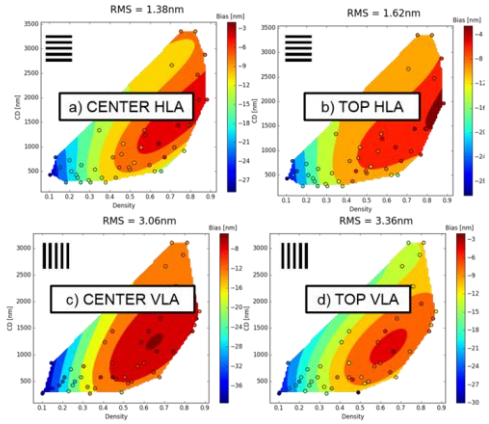

Figure 2: Interpolation functions of the bias measured between the master and the imprint for vertical and horizontal lines located at the center and the top of the wafer

The bias was evaluated by measuring the dimensions on the master and corresponding ones on the imprint for 48 selected features. The difference is then interpolated by drawing the critical dimension (CD) versus pattern density (Fig 2.). The same approach applied for the pitch has revealed an influence of the features orientation on the bias. Finally, we demonstrated that the bias can be reduced to less than 2 % for low density patterns [2].

Perspectives
The bias modelling induced by NIL is specific to this technology. As the proposed models assume that the process signatures are repeatable imprint after imprint, the next step is to define design rules to take into account the cumulative bias with simple linear models.

RELATED PUBLICATIONS:
[1] H. Teyssedre et al. Proceedings Volume 10032, 34th European Mask and Lithography Conference, 2018, http://dx.doi.org/10.1117/12.2326106
[2] F. Delachat et al., Proceedings of SPIE, 2018, https://doi.org/10.1117/12.2298407

Multibeam Lithography: Process Integration Flow and Associated Metrology

RESEARCH TOPIC:
Electron beam lithography, security, metrology

AUTHORS:
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ABSTRACT:
The maskless electron beam lithography system is a cost-effective patterning solution, complementary to optical lithography, for a wide range of technologies, from mature nodes down to 28 nm.
In 2018, CEA-Leti and Mapper Lithography have demonstrated a low-cost cybersecurity breakthrough that allows encrypting unique codes directly on individual chips. MAPPER Lithography has introduced its first functional prototype, the FLX–1200 platform at CEA-Leti, which is designed to reach throughput of one 300mm wafer per hour (wph).

SCIENTIFIC COLLABORATIONS: MAPPER Lithography BV, SCREEN, STMicroelectronics, KLA, NOVA

Context and Challenges
The FLX-1200 exposure tool offers a huge panel of competitive advantages, such as cost of ownership benefit, high-resolution potential and full writing flexibility opportunity to address the increasing demand for hardware-secure solutions to prevent chip cloning.
The main challenge to overcome for multibeam maskless lithography technology's suitability is the insertion in existing silicon-chip manufacturing directly on product wafers manufactured in a conventional IC fab and secondly to measure and monitor metrology parameters such as overlay and stitching for each individual beams.

Main Results
CEA-Leti and MAPPER Lithography produced a unique competence-and-technical combination for data preparation, proximity-effect corrections, tool monitoring, metrology and etch-transfer processes. A complete integration process flow was demonstrated, compliant with industrial specifications for the IC CMOS 40nm-node logic, including specific process steps
• Clamping of wafer coming from external IC fab at VIA3 level
• Customer design transfer on the machine without errors
• Reading alignment marks created with standard optical scanner and alignment on the buried layer and exposing the layout of real products [1] (Fig. 1).

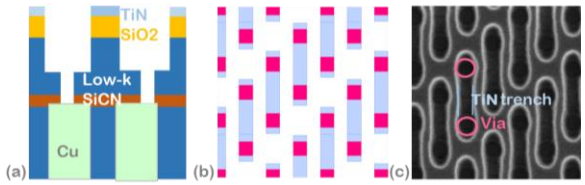


Figure 1: Pattering demonstration on first customer 300 mm wafer exposed with FLX-1200 multi beam tool at 5 kV (a) VIA3 stack (b) IC cell layout (c) SEM image after etch transfer showing alignment of 2nd litho/etch of holes in the dielectric printing on multibeam tool on 1st litho/ etch of TiN line exposed on immersion scanner

One of the metrology challenges for massively parallel electron beams is to measure overlay and stitching for each individual beams, that is per 2 µm wide stripes. In 2018, CEA-Leti made breakthrough advances in this direction, working in two different fields:
• Image based overlay measurement [2], in partnership with KLA (example on fig. 2),
• Scatterometry on non-uniform gratings for CDU defects per beam, in partnership with Nova Instruments [3].

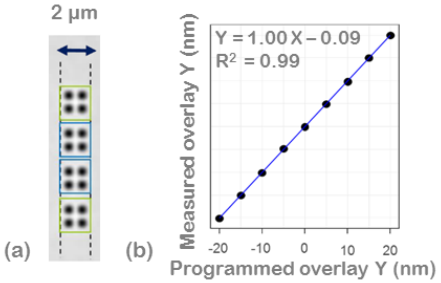
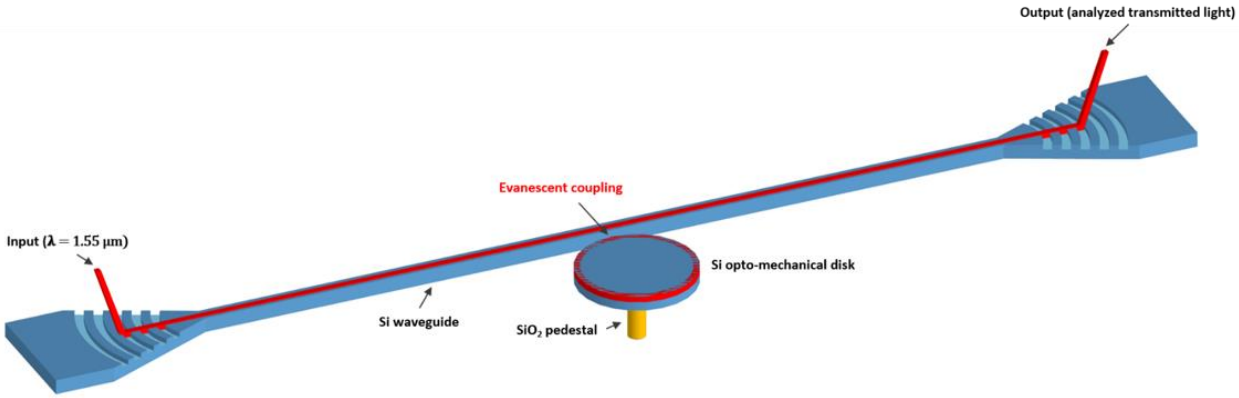


Figure 2: (a) Overlay target measured with OVL tool Archer 600, having a width of only 2.2 µm (b) Correlation of the targets with programmed overlay resulting in a measure-and-move (MAM) time of 0.35 s and a total measurement uncertainty (TMU) of 0.3 nm.

The best performing overlay targets were incorporated in an exposure. Preliminary results of one overlay target shows an excellent correlation to programmed overlay (Fig. 2).

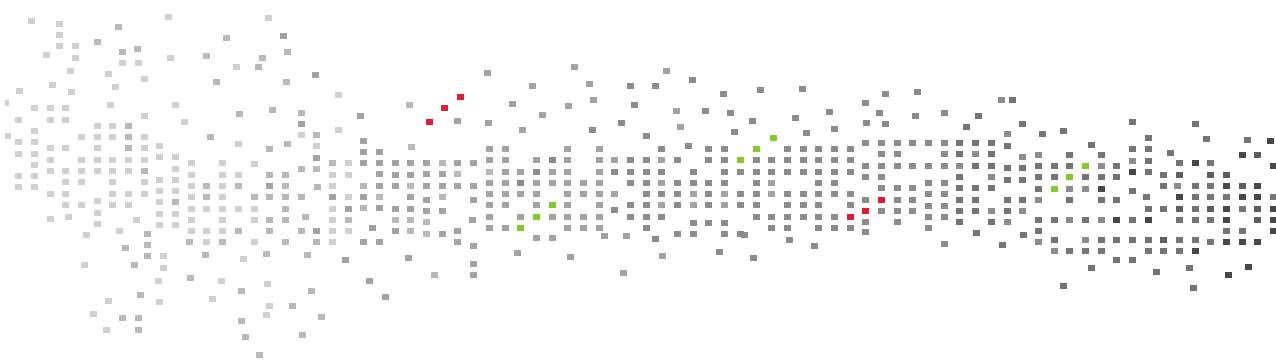
Perspectives
To further the platform's maturity, we will pursue improvements to the hardware. CEA-Leti intends to extend the overall demonstration program to highlight the capability of this technology to fully meet industry needs. This activity of cyber-security represents a clear technology path for the manufacturing of tomorrow's devices.

RELATED PUBLICATIONS:
[1] I. Servin et al, Proceedings of SPIE, 2018, https://doi.org/10.1117/12.2297162
[2] G. Rademaker et al., Proceedings of SPIE, 2018, https://doi.org/10.1117/12.2297535
[3] G. Rademaker et al., EMLC, 2018, https://doi.org/10.1117/12.2326595


Output (analyzed transmitted light)
Evanescent coupling
Input (λ = 1.55 µm)
Si opto-mechanical disk
Si waveguide
SiO2 pedestal

04 MEMS, NEMS& RF COMPONENTS

- **Neutral Mass Spectrometry**
- **Optomechanical Resonators in Liquid for Biosensing**
- **Optomechanical AFM Probes**
- **A New 3D Process Adapted to High Performance Capacitive Inertial Sensors**
- **Sensor Bandwidth Tuning**
- **PZT Properties**
- **Piezoelectric Devices**



Neutral Mass Spectrometry

RESEARCH TOPIC:

NEMS, mass sensing, resonators, biological applications

AUTHORS:

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ABSTRACT:

Measurement of the mass of particles in the mega- to gigadalton range is challenging with conventional mass spectrometry. Although this mass range appears optimal for nanomechanical resonators, nanomechanical mass spectrometers often suffer from prohibitive sample loss, extended analysis time, or inadequate resolution. We have demonstrated a system architecture combining nebulization of the analytes from solution, their efficient transfer and focusing without relying on electromagnetic fields, and the mass measurements of individual particles using nanomechanical resonator arrays. This system showed high detection efficiency and effectively performed molecular mass measurements of bacteriophage T5 capsids with masses up to 105 megadaltons.

SCIENTIFIC COLLABORATIONS: CEA BIG, CEA INAC, I2BC

Context and Challenges

Prior NEMS-based mass spectrometry systems were based on conventional MS systems including ionization and ion guides. They cumulated losses due to ionization, collection and ion transfer, as well as the miniscule active area of nanomechanical resonators. We developed here a new architecture dedicated to massive particles, avoiding ionization altogether, with a nebulization stage, a focusing stage and an array of nanomechanical resonators to increase the detection efficiency.

Main Results

Arrays of nanomechanical resonators comprised 20 individual resonators. The readout of a whole array is performed in typically 100 ms without degrading the performance compared to individual nanoresonators [1]. We first characterized the new system (Fig. 1) with 30 MDa polystyrene nanoparticles.

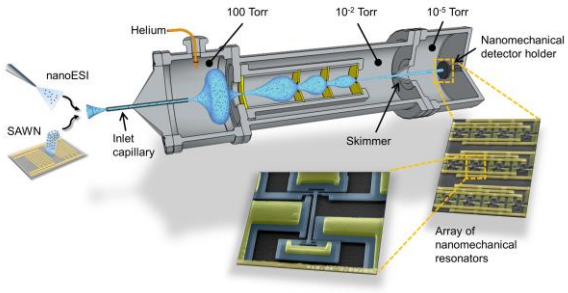

Figure 1: Neutral mass spectrometry system based on nanomechanical resonator array.

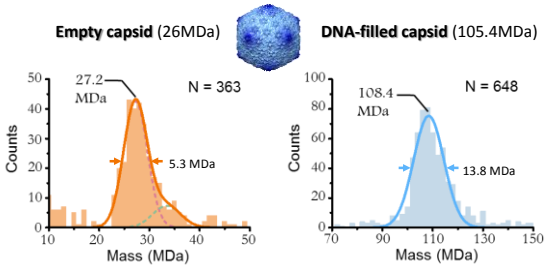

Figure 2: Obtained mass spectra of bacteriophage T5 capsids

We showed we could determine their mass with high efficiency, 5 orders of magnitude larger than previous NEMS-based systems using ion guides. We then performed measurements of capsids of bacteriophage T5 viruses with and without their genome content. Unlike PS NPs, empty and filled capsids have well-defined molecular masses, calculated to be 26.0 and 105.4 MDa, respectively (Fig. 2). The measurements are very close to expected masses and are the highest molecular mass measured with mass spectrometry [2].

Perspectives

The system is now fully functional and routine measurements can be performed. Inorganic and biological particles are now under study. Arrays of more than 1000 resonators co-integrated with CMOS are currently under test and will decrease the analysis time from a few hours to a few minutes. Single-particle mass sensing with optomechanical resonators is being developed right now so particles of any size, shape, aspect ratio can be analyzed.

RELATED PUBLICATIONS:

[1] E. Sage *et al*, Nature Communications 2018, DOI: 10.1038/s41467-018-05783-4
[2] S. Dominguez-Medina *et al*, Science 2018, DOI: 10.1126/science.aat6457

Optomechanical Resonators in Liquid for Biosensing

RESEARCH TOPIC:
Micro/Nano-gravimetry, Optomechanics, Biological sensing, BioMEMS, Biological functionalization, Thermomechanical noise

AUTHORS:
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ABSTRACT:
We report the first VLSI process for silicon based optomechanical resonant microdisks on 200 mm silicon wafers. Optical characterization demonstrated optical quality factors in excess of 1 million. With such performance, 10^{-17} m.Hz $^{(-1/2)}$ displacement resolution was demonstrated and the brownian motion of the microdisks were resolved in both air and water. This allowed for first biosensing experiments.

SCIENTIFIC COLLABORATIONS: Institut de biologie intégrative de la cellule (I2BC-CNRS), Laboratoire MPQ Paris Diderot

Context and Challenges
On-chip optomechanics has been a privileged route towards fundamental studies in the last 15 years and it has recently become mature enough to reach a more applied realm. Sensing experiments with optomechanical resonators are still uncommon, and VLSI were still to be demonstrated. Moreover, a sensitive resonator for mass sensing directly immersed in liquid has eluded research for many years.

Main Results
Optomechanical system performance depends both on the coupling between the optical and the mechanical resonators and on the optical cavity, which needs to be finely optimized. We have developed a VLSI-compatible process to optimize the performance of optical cavities like silicon optomechanical microdisks. The devices were the first optomechanical resonators fabricated on 200 mm SOI wafers with variable shape beam lithography, allowing for both high fabrication throughput and high patterning resolution: each wafer contained more than 120,000 optomechanical devices. Most measured loaded quality factors were in the high 100,000s, and many resonances showed quality factors above 1 million. These figures are among the best measured in the literature with silicon disks of a few µm radius. We were able to resolve the thermomechanical motion of our resonators at a few 100 MHz frequencies at ambient pressure without the need for an optical amplifier, demonstrating motional sensitivity down to 10^{-17} m.Hz$^{(-1/2)}$.
Following a recent experiment, we first showed that our silicon VLSI microdisks retained high optical performance in liquid, as well as exquisite motional sensitivity. Next, we performed the first biosensing demonstration with optomechanical resonators directly immersed in liquid: after surface functionnalization, proteins and viruses were detected in liquid at very low concentrations. These demonstrations, along with our first multiplexed optomechanical resonators, show that VLSI optomechanics is a viable route for sensing.

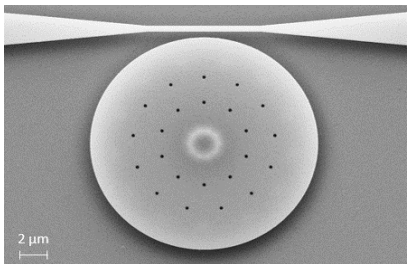


Figure 1: SEM micrograph detail of a 12 µm large optomechanical microdisks.

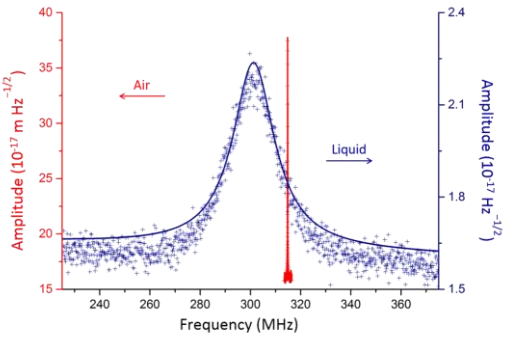


Figure 2: Mechanical resonance spectra of the mechanical motion of the optical microdisks in air and liquid. Actuation of motion is realized through thermal fluctuations of the microdisk itself

Perspectives
Our efforts are now dedicated to replicate biological detection with other target/bioreceptor pairs. We seek improvement of our limit of detection through a better actuation and transduction of our resonant microdisks.

RELATED PUBLICATIONS:
[1] M. Hermouet *et al*. SPIE BIOS Proceedings vol. 10491, (2018). DOI: 10.1117/12.2290322
[2] M. Hermouet *et al*. IEDM Proceedings in 12.4.1–12.4.3 (2018). DOI: 10.1109/IEDM.2018.8614532
[3] M. Hermouet *et al*. IEEE MEMS Procedings. 844–845 (2018). DOI: 10.1109/MEMSYS.2018.8346687

Optomechanical AFM Probes

RESEARCH TOPIC:
AFM probe, high speed AFM, Optomechanics, force sensor, resonant sensor, silicon photonics, non-contact interaction

AUTHORS:
G. Jourdan, M. Gely, S. Hentz, M. Hermouet, (P-E. Allain), (L. Schwab), (B. Legrand), (I. Favero), (M Faucher), (B. Walter)

ABSTRACT:
A VLSI optomechanical micro-resonator has been designed to address high resolution and high speed AFM Imaging. The mechanical resonance frequency of the probe is above 100 MHz with a Q-factor of 1 000 in air, yielding a measurement bandwidth above 100 kHz. Low thermomechanical noise floor has been resolved with exquisite motion detection limit down to a few 10^{-16} m.Hz$^{-0.5}$, thus allowing very low oscillation amplitudes down to a few tens of pm. This is essential to probe molecular interactions at such a scale. This performance, enabled by optomechanical transduction, paves the way for very high-speed and ultra-sensitive various sensing applications, beyond AFM field.

SCIENTIFIC COLLABORATIONS: LAAS, MPQ, IEMN

Context and Challenges
Scanning probe microscopy has been a major instrumental breakthrough for the study of physical, chemical and biological phenomena at the nanoscale. In particular, atomic force microscopy (AFM) is able to provide sample morphology down to the atomic scale. For more than 20 years, boosting the scan rate of AFM has been an increasingly difficult challenge. However still today, performing user-friendly AFM studies at video rate remains unreachable in most cases. Conventional AFM probes based on micro-sized cantilevers is the major obstacle in terms of bandwidth and sensitivity.

Main Results
Optomechanics has been an emerging transduction mean for the last fifteen years. It allows large bandwidth (>GHz) and high sensitivity (< 10^{-17}m/$\sqrt{Hz}$) capabilities as well as on chip integration to address Micro / Nanomechanical Systems. In this work, a fully optically operated resonating optomechanical atomic force probe with a frequency larger than 100 MHz, two decades above the fastest microscope cantilevers, has been fabricated to enable fast AFM imaging [1,2].

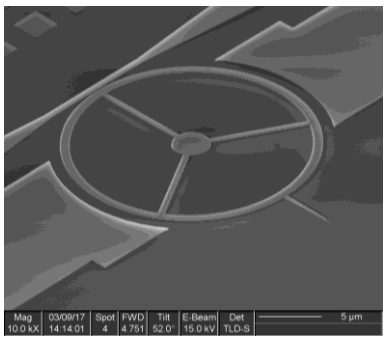


Figure 1: SEM Image of an optomechanical AFM probe before substrate etching below the tip area.

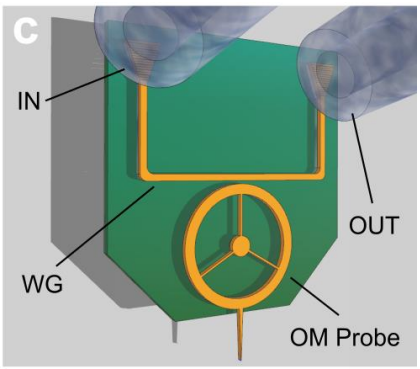


Figure 2: Schematic of an optomechanical AFM chip that can be integrated inside an AFM head. The photonic circuit is fed with a laser beam by two out of plane optical fibers.

The probe, depicted in Fig. 1, consists of a suspended silicon ring, on which a tight tip has been clamped. The photonic cavity is coupled to a silicon waveguide, which can itself be coupled with two optical fibers (Fig. 2). A dedicated etching process is under development to obtain an overhanging tip outside the substrate, thus allowing the probe to reach a sample surface. Approach-retract experiments have demonstrated the large bandwidth of the device and its capabilities to probe molecular interactions at the close vicinity of a surface [3]. Oscillation amplitudes can indeed be kept below tens of pm, well below usual AFM probes around 1 nm.

Perspectives
Optomechanical AFM probes are a promising tool to study biological systems like proteins, virus, etc. It provides a way to push AFM imaging to high-speed analysis of biological properties of these species. In particular, ultra-fast force spectroscopy is expected to deliver valuable information about the relation between their conformation and their function.

RELATED PUBLICATIONS:
[1] B. Legrand et al. AVS 65th International Symposium & Exhibition, Oct 2018, Long Beach, United States, Invited talk. https://hal.laas.fr/hal-01908666
[2] L. Schwab et al. IEEE International Electron Devices Meeting (IEDM), Dec 2018, San Francisco, United States. DOI: 10.1109/IEDM.2018.8614508
[3] P.E. Allain et al. ArXiv:1810.06209, https://export.arxiv.org/abs/1810.06209

A New 3D Process Adapted to High Performance Capacitive Inertial Sensors

RESEARCH TOPIC:
MEMS - Inertial - 3D process - capacitive detection

AUTHORS:
F.Maspero, S.Delachanal, A.Berthelot, L.Joet, (V. F. López-Rey), (G.Langfelder) and S.Hentz

ABSTRACT:
A new process for multi-layer MEMS has been developed and used to design an in-plane accelerometer. With this solution, sensing elements (here, comb-fingers) and seismic mass can be fabricated in different layers and located on top of each other for a significantly reduced footprint and enhanced performance: both can be independently optimized. For this first demonstration, we show an intrinsic noise floor of 7 µg/√Hz, mechanical stiffness of 20 N/m, large bandwidth and a sensitivity of 5.3 fF/g with a total footprint of 400 µm x 600 µm.

SCIENTIFIC COLLABORATIONS: Politecnico di Milano, Italy

Context and Challenges
In most capacitive MEMS inertial sensors, the seismic mass and sensing elements are patterned in the same silicon layer. A thick layer increases seismic mass and decreases the Brownian noise floor, whereas a thin layer enables smaller gaps between electrodes and decreases electrical noise.
This new technology overcomes this tradeoff by providing two layers, a thin one and a thick one. It enables submicronic comb fingers and large mass on top of each other. This technology has been tested with in plane accelerometer designs (Figure 1), where submicronic gaps made surface variation detection relevant.

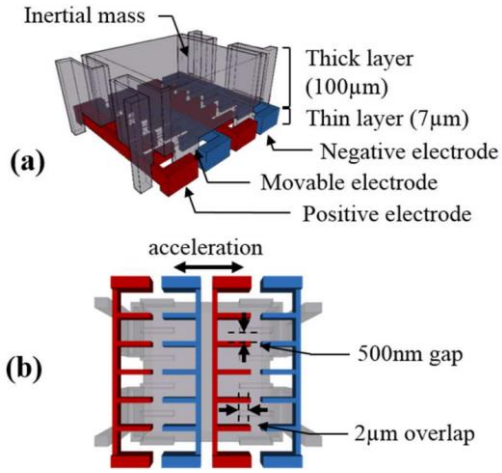


Figure 1: (a) schematic view of a 2-layer in-plane accelerometer (b) details of the comb fingers, critical dimensions.

Main Results
A first run has been successfully processed and delivered functional devices. Figure 2 shows the thin layer side of a 400µm x 600µm in plane accelerometer.

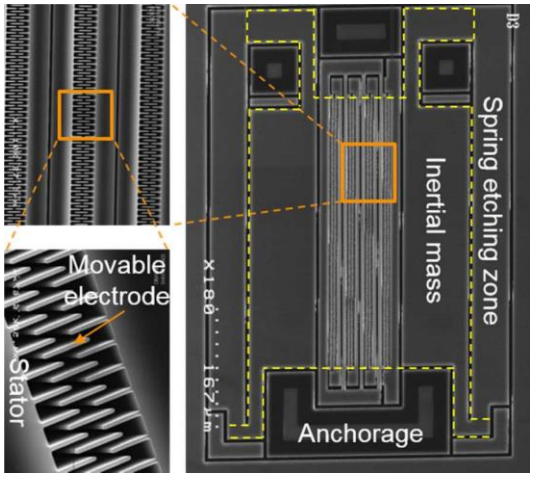


Figure 2: SEM images of the thin layer of a device

This device presents a 146 dB dynamic (on 1 Hz), exceptional performance for an open loop readout accelerometer. It combines multiples advantages:
- ✓ High linearity due to surface variation (full scale = 190g).
- ✓ High sensitivity due to 500 nm gap comb fingers (5.3 fF/g).
- ✓ Low Brownian noise due to 100 µm thick mass (7 µg/√Hz).

Moreover, the 4.8 kHz resonant frequency provides a large bandwidth and high stiffness prevents for sticking.

Perspectives
Addressing the out-of-plane detection is the next step. Surface variation detection in this direction is challenging but this 3D process provides solutions.
It would be also interesting to use this technology on other sensors, such as gyroscopes.

RELATED PUBLICATIONS:
[1] F. Maspero et Al., IEEE Micro Electro Mechanical Systems (MEMS) conference, 2018, 10.1109/MEMSYS.2018.8346495
[2] F. Maspero et Al., IEEE International Symposium on Inertial Sensors and Systems (INERTIAL) conference, 2018, 10.1109/ISISS.2018.8358139

Sensor Bandwidth Tuning

RESEARCH TOPIC:
MEMS, MEMS accelerometer, electromechanical coupling

AUTHORS:
B. Fain, F. Souchon, A. Berthelot, R. Anciant, P. Robert and G. Jourdan

ABSTRACT:
Some specific requirements of high-performance accelerometers, such as a good robustness in a harsh mechanical environment, require advanced design. At LETI, we developed a strategy to tune the performance of a MEMS accelerometer packaged in vacuum, so that accelerometers and gyrometers can be fabricated within the same process flow. A large electromechanical coupling between the MEMS and a dissipative resistor is used to adjust the mechanical parameters of the accelerometer. By this means, the resonance of the accelerometer can be suppressed in vacuum, or, alternatively, the bandwidth of the sensor can be increased. This also opens interesting development tracks for vacuum-sealed accelerometers, such as dynamic tuning of the mechanical parameters.

Context and Challenges

In the last decade, an important focus has been made on low-cost inertial sensors for the consumer market. Yet, specific needs such as a good robustness in vibrating environment cannot be achieved with such sensors and require advanced design and processing. In particular, the fabrication of both accelerometers and gyrometers on the same process flow is a challenging task, since gyrometers require vacuum packaging, which impede the performance of accelerometers usually damped by squeeze-film effects. For this purpose, we developed an alternative strategy, the electromechanical coupling of a MEMS accelerometer with a dissipative resistor, to tune the bandwidth and to suppress the resonance of an accelerometer operated in vacuum.

Main Results

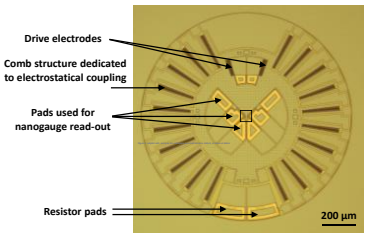


Figure 1: Optical picture of the M&NEMS accelerometer. The built-in resistors are located below the resistor pads.

The MEMS accelerometer has been designed, fabricated and tested in LETI facilities. The device is based on a rotating structure with piezoresistive detection (Fig. 1) [1]. Compared with previous works, two additional structures located on the edge of the seismic mass form two variable capacitors to ensure the electromechanical coupling. Both capacitors are polarized with a DC voltage. This induces a feedback at the electrode stage when the mass is moving, that may be described by an additional damping to the structure, and, more surprisingly, by an additional negative mass that reduces the effective mass of the device [2]. The mechanical response of the accelerometer has been studied in vacuum (1 mbar), for different polarization voltages V_{EM} (Fig. 2). When V_{EM} is increased, the resonance is progressively suppressed and the bandwidth is also increased, which is consistent with the theoretical expectations. The measurements demonstrate an efficient feedback, which is achieved thanks to built-in resistors that drastically reduce the impact of parasitic capacitances

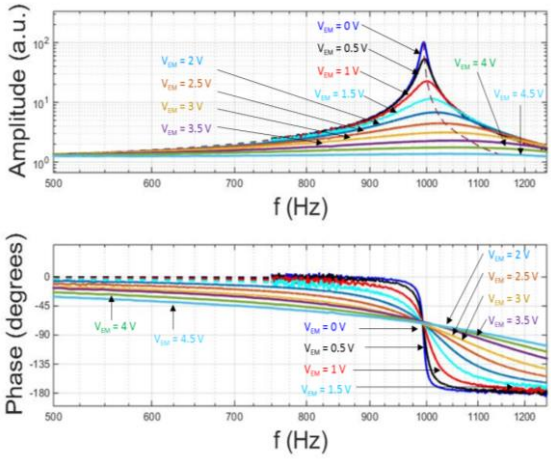


Figure 2: Frequency response of the accelerometer as a function of V_{EM}, measured at 1 mbar.

Perspectives

Such a control of the mechanical parameters of the accelerometers presents interesting development possibilities, such as the dynamic tuning of the accelerometer, before and during operation.

RELATED PUBLICATIONS:
[1] B. Fain et al, IEEE Inertial Sensors 2018, 10.1109/MEMSYS.2018.8346714
[2] B. Fain et al, IEEE MEMS 2018, 10.1109/ISISS.2018.8358142

PZT Properties

RESEARCH TOPIC:

PZT, operando measurements, ferroelastic switching and relaxation, dielectric, ferroelectric, pyroelectric and piezoelectric applications

AUTHORS:

G. Le Rhun, I. Gueye, D. Cooper, O. Renault, N. Barrett, B. Allouche, P. Gergaud, N. Vaxelaire, F. Casset, S. Fanget (A. Devos, P. Emery, E. Defay)

ABSTRACT:

We aim at better understanding correlations between physicochemical, structural and electrical properties of Lead Zirconate Titanate (PZT) thin film in order to ease and optimize its integration in Metal-Insulator-Metal (MIM) structures for piezoelectric, pyroelectric and dielectric applications. Using various advanced characterization techniques such as Hard X-ray photoelectron spectroscopy (HAXPES), TEM, in-situ XRD or picosecond acoustics (PA), we were able to highlight several phenomena such as the benefit of post metallization annealing (PMA) on PZT capacitors performances, ferroelastic switching under external electric field that contributes to piezoelectric effect, but also ferroelastic domain wall relaxation in the GHz range.

SCIENTIFIC COLLABORATIONS: MENAPIC (Lille), IEMN (Lille), LIST (Luxembourg)

Context and Challenges

Pb(ZrxTi1−x)O3 (PZT) material is an ideal candidate for applications such as piezoelectric actuators, infrared pyroelectric detectors, and decoupling capacitors. The common basic structure for all those applications is a MIM capacitor. In order to optimize performances, one needs to understand both PZT material and PZT capacitor behaviors in conditions similar to real-life operating conditions. This can be done through operando measurements. It allows direct correlations between structural and electrical properties.

Main Results

PMA at 550°C was shown to improve electrical performances of PZT based MIM structures, in particular the breakdown field, and eliminates imprint, thus leading to symmetric ferroelectric response curves (Fig. 1). Those effects were correlated with the physical chemistry of top electrode/PZT interface probed by HAXPES (operando) and TEM. We concluded there may be a quite narrow thermal budget window for PMA to provide enhanced electrical characteristics without inducing irreversible chemical changes [1].

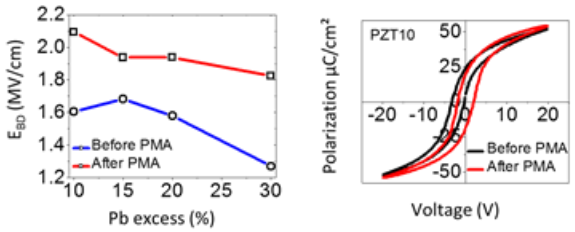


Figure 1: Effect of PMA on various electrical properties of PZT film with lead excess comprised between 10% and 30%.

Over the past few years, operando characterization techniques of functional thin films have been developed at LETI, mainly using synchrotron radiations. We presented a set-up using a laboratory X-ray source to investigate functional thin films under electric field [2]. It was able to probe domain switching in ferroelectric tetragonal PZT thin films (Fig. 2). The relevance of such a set-up is demonstrated by the ability to separate the existing contributions to macroscopic piezoelectric coefficient (lattice strain and domain wall motion).

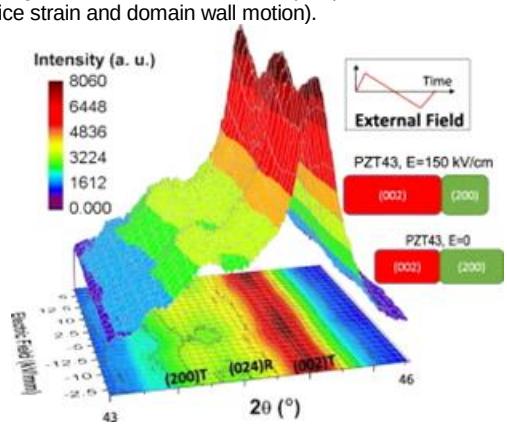


Figure 2: evolution of ferroelastic domains (switching between *a* and *c* tetragonal domains) of PZT as a function of external electric field.

In collaboration with MENAPIC, we presented a method, mostly based on Picosecond Acoustics, to perform elastic measurements on a thin-film as a function of frequency in the GHz range. It was applied to a PZT thin film for which a 9% increase in the longitudinal sound velocity was measured above 20 GHz. This was interpreted as a direct observation of the ferroelastic domain wall relaxation [3].

Perspectives

In-Operando measurements, using laboratory X-ray sources, will be used more systematically for investigating functional thin films under real operational conditions. Modified PA technique could be used as a generic characterization mean to identify phase transitions of materials over the whole GHz range.

RELATED PUBLICATIONS:

[1] I. Gueye et al., Applied Physics Letters, 113, 132901, 2018, DOI : 10.1063/1.5041767
[2] B. Allouche et al., Materials and Design 154, 340–346, 2018, DOI : 10.1016/j.matdes.2018.05.016
[3] A. Devos et al., Applied Physics Letters, 112, 262905, 2018, DOI: 10.1063/1.5035479

Piezoelectric Devices

RESEARCH TOPIC:
Piezoelectric actuator, applications, micro-mirror, haptic, biologic

AUTHORS:
F. Casset, B. Neff, JS. Danel, B. Desloges, S. Fanget, P. Poncet, V. Agache, M. Colin, (A. Latour), (A. Millet)

ABSTRACT:
Thin-film piezoelectric actuators are well suited to MEMS devices. The CEA has developed for several years a strong expertise in thin-film piezoelectric materials and technologies. We already developed various MEMS devices using thin-film AlN, PZT or Electro Active Polymer (EAP) actuators. In particular, we demonstrated the possibility to control specific patterns of a liquid by the use of mechanical vibration modes of a PZT actuated MEMS membrane. We also developed a resonant asymmetric micro-mirror using a thin-film EAP material as the actuator, for a low temperature actuator process. Finally, we demonstrated the concept of a haptic effect obtained using a polymer technology and EAP actuators, for low cost and large area devices.

SCIENTIFIC COLLABORATIONS: LAB4MEMS2 and Happiness projects, DCOS/DTBS, INSERM CEA/LITEN

Context and Challenges
Piezoelectric actuators are well suited to MEMS devices such as micro-mirrors, haptic interfaces or lab-on-chip systems. The CEA has developed for several years a strong expertise in thin-film piezoelectric materials and technologies. In particular, we present a lab-on-chip system based on Pb(Zr0.52, Ti0.48)O3 (PZT) actuators, which are an integrated and low power solution to study biological cells. We also present a resonant asymmetric micro-mirror and a haptic interface using innovative Electro Active Polymer actuators for low cost and large area devices.

Main Results
Vibrating MEMS can address a large domain of applications in microfluidics and biology. In particular, they offer the possibility to control fluid flow inside a fluidic cavity and allow the creation of positions of stability where flowing particles tend to stay. This offers outstanding interest concerning manipulation of living cells. We proved the possibility to control specific patterns of the liquid by the use of the mechanical vibration modes of a PZT actuated MEMS membrane (Fig. 1) [1]. Developments are ongoing to study adhesive living cells and how to relate their biophysical properties with any variations of the membrane modes.

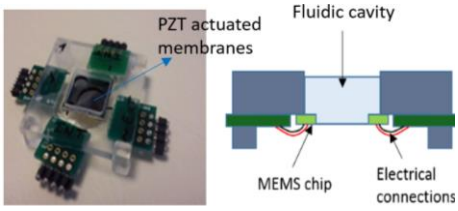


Figure 1: Photography and schematic cross section of the Lab-on-chip system based on PZT actuators [1].

Piezoelectric actuators can also actuate a micro-mirror able to guide or deflect an optical beam or a laser. This element is a key component for optical applications such as micro-scanners, pico-projectors or LIDAR systems. We developed a resonant asymmetric micro-mirror using a thin-film Electro Active Polymer (EAP) material as the actuator (Fig. 2). We measured an interesting optical scan angle of 10° using only 30V_{rms} [2]. This opens the way for innovative low cost and low temperature process piezoelectric actuators.

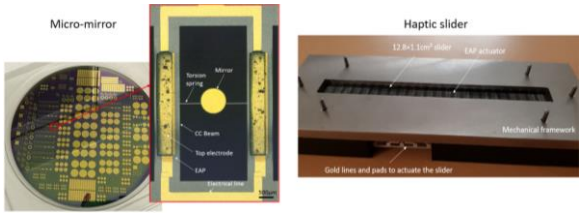
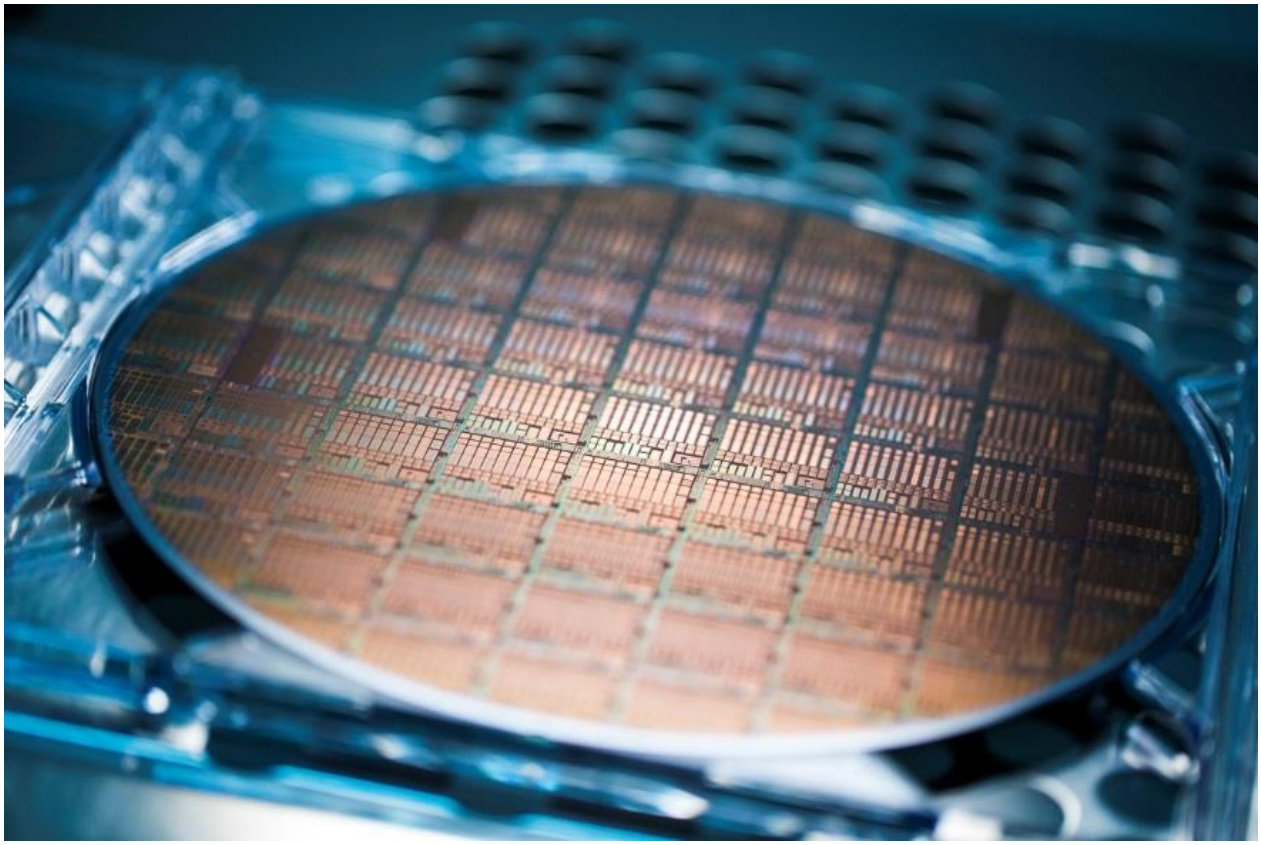


Figure 2: Resonant asymmetric micro-mirror and haptic slider using Electro Active Polymer actuators [2, 3].

Finally, piezoelectric actuators are well adapted to develop haptic devices, which allow the user to interact with their environment by the sense of touch. We used an all-polymer technology and EAP actuators to develop a haptic slider based on the surface roughness modulation induces by an ultrasonic vibration of the device (Fig. 2). It consists in changing the friction between the finger and the resonating slider. It provides a high granularity level of haptic sensation. Electromechanical characterization of the haptic slider, in good agreement with modelling, shows a displacement amplitude of 2.2µm at 19.6 kHz and 70V, leading to a haptic sensation for the user [3].

Perspectives
Piezoelectric actuators are well adapted for several applications. We already developed various MEMS devices using thin-film AlN, PZT or EAP actuators. A collective process to integrate bulk piezo ceramic actuators is currently under development to provide piezoelectric actuator solutions for a large number of MEMS industrial applications.

RELATED PUBLICATIONS:
[1] B. Neff et al., EuroSime, 2018, DOI:10.1109/EuroSimE.2018.8369876
[2] F. Casset et al., IEEE Conference on Sensors (Sensors), 2018, DOI:10.1109/ICSENS.2018.8630286.
[3] F. Casset et al., Micromechanics and Microsystems Europe workshop (MME), 2018.



05 POWER & ERNERGY

- GaN-on-Si Power Roadmap
- Thin Film Batteries
- Advanced Reliability Testing of GaN-on-Si devices
- Characterization and Optimization of III-N Materials for Power Electronics Applications
- New Thin Film Materials for Microbatteries

GaN-on-Si Power Roadmap

RESEARCH TOPIC:
GaN, converters, normally-off, HEMT, MOSCHEMT, CMOS compatible

AUTHORS:
L. Di Cioccio, E. Morvan, Y. Baines, A. Torres, T. Bouchet

ABSTRACT:
The main objective in the LETI power electronic roadmap is the miniaturization of power converters to increase the energy efficiency of the systems while reducing the cost. It is also important to improve reliability and ensure operation at higher temperatures (300 °C), with the markets of automotive (electric vehicles and hybrid-electric vehicles) and motor drives for industrial tools being targeted. To achieve these objectives for power converters from a few watts to several hundred of kilowatts, it is essential to increase their operating frequency.
GaN-on-Si power devices are capable of responding to these requirements because GaN material allows high frequency switching (several MHz) and a higher power density than silicon material (10 times greater). Furthermore, 200 mm GaN-on-silicon enables CMOS compatible technology leading to lower cost and improved robustness of the process.

Context and Challenges
The commercially available solution to make normally-off GaN high electron mobility transistors (HEMTs) is pGaN gate architecture. P-type GaN makes pGaN an outstanding gate metal for depleting the channel beneath the gate. However, this device architecture suffers from a tradeoff between the threshold voltage and the channel sheet resistance.

Main Results
LETI has chosen to develop MOS-channel HEMT (MOSCHEMT) GaN architecture, fabricating 'normally-off' devices which give functionality similar to a classic silicon based MOS, aiming to break the aforementioned tradeoff. Our roadmap [1] consists of a system on chip (SoC) route towards monolithic solutions for low and mid power applications and a route towards system in package (SiP) (Fig. 1), with five main axes of work: epitaxy, devices, passives, co-integration, and system architectures.

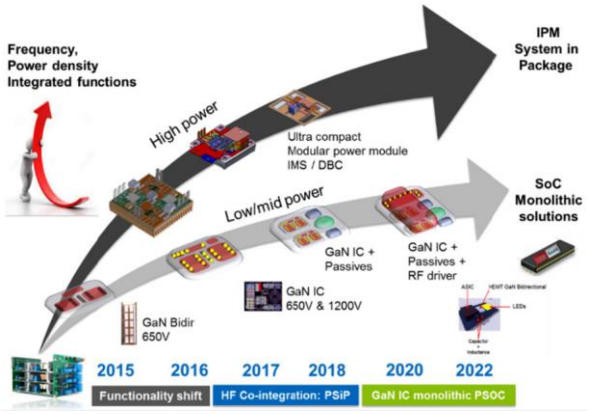


Figure 1: Power systems roadmap at Leti. A SoC route towards monolithic solutions is important for miniaturization for low and mid power solutions. For higher voltages, a SiP route is preferred [1].

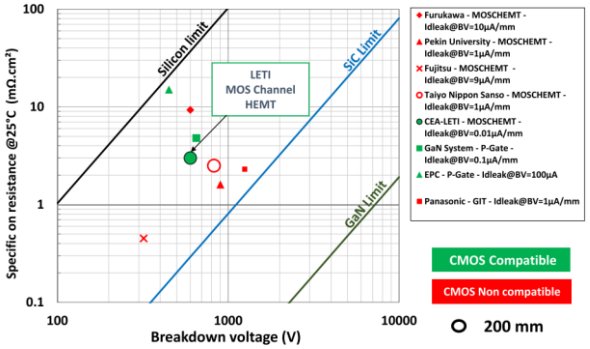


Figure 2: Leti shows unique 200 mm, CMOS compatible GaN devices with equivalent GaN device performance.

Best-in-class results have been already published (Fig. 2) and allows to converge on the heart of this technology being the integrity of the MOS gate; a challenge that Si and SiC have already faced in the past. Several ingredients have to be co-developed to target efficient MOSCHEMT: simulation, including first principle calculation (*i.e.* interface chemistry and physics); device technology constant improvement through epitaxy [2] and interface management; device characterization and reliability (*i.e.* beyond JEDEC standards toward zero fault detection).

Perspectives
The use of GaN-on-Si as a substrate for high power transistors is becoming an increasingly common choice, as an affordable large area alternative to expensive bulk substrates. Although there are still significant challenges to be overcome in order to produce high quality devices on these substrates, GaN devices will take full advantage of both the remarkable properties of GaN, and of CMOS compatible fabrication plants, such as the one at Leti, to achieve high performance and low cost devices.

RELATED PUBLICATIONS
[1] H. Amano *et al*., Journal of Physics D, 2018, https://doi.org/10.1088/1361-6463/aaaf9d
[2] M. Charles *et al*., High Mobility Materials for CMOS Applications, 2018, https://doi.org/10.1016/B978-0-08-102061-6.00004-5

Thin Film Batteries

RESEARCH TOPIC:
Thin film, batteries, transparent battery, on-chip energy, solid state, LiPON, free form factor

AUTHORS:
S. Oukassi, L. Baggetto, C. Dubarry, L. Le van Jodin, S. Poncet, R. Salot

ABSTRACT:
Electrochemical energy storage devices have attracted extensive attention for the power supply of next-generation electronics. In this paper, free form factor and structural miniaturized thin film batteries have been fabricated using specific designs and microfabrication techniques in order to achieve high electrochemical performance $LiCoO_2$/LiPON/Si devices. While reported studies are limited to battery structures involving liquid or polymer materials, our devices will contribute to improve form factor freedom, extend operating ranges, enhance long-term stability, and will be relevant to the integration into various micro and nanoelectronic devices.

Context and Challenges

Novel multifunctional electronic devices related to the Internet of Things (IoT) and wearables are becoming increasingly important in our daily life. These miniaturized electronic devices no longer require a conventional, bulk, energy storage device. Instead, a power source that can be perfectly integrated within the overall architecture, and that can ensure an additional structural function has become crucial. Thin film batteries (TFBs) are considered as one of the most promising candidates to meet a wide range of application requirements since they offer high energy/power densities and free form factor design opportunities.

Main Results

A first demonstration has been achieved with free form structural transparent TFBs (grid-structured design) on glass substrates with dimensions below the resolution of the human eye [1]. Transmittance up to 60 % have been measured for the obtained TFBs. Discharge capacity as high as 0.15 mAh has been recorded upon C/2 cycling rate (Fig. 1).

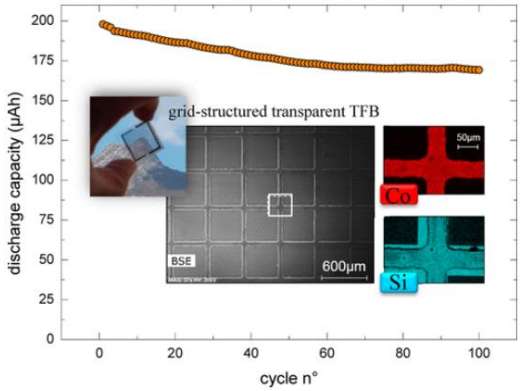


Figure 1: Transparent TFBs: grid structure (SEM, EDS mapping) and capacity variation during cycling. [1]

A second demonstration consisted on realizing biomimetic shaped (dragonfly abdomen) TFBs for powering MEMS actuation based micro/nanorobotics. The final structures presented a total mass of approximately 60 mg per cm² of active area, with a mean overall thickness of 100 µm. Experimental results of TFB cycling at different C rates showed almost no capacity fade for current densities between 0.5 and 10 mA, leading to surface energy densities as high as 0.15 mWh.cm^{-2} and power densities up to 5 mW.cm^{-2}.

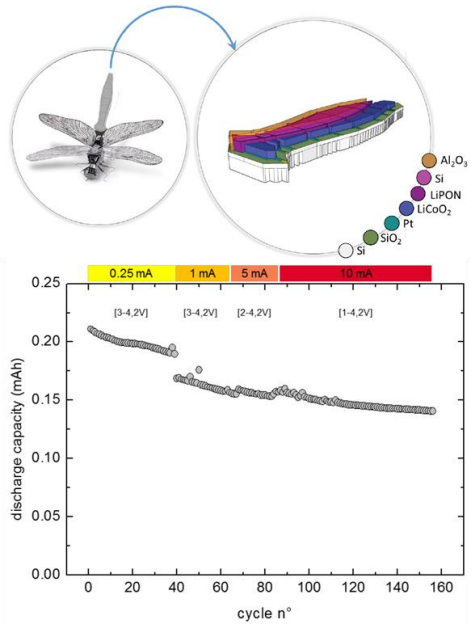


Figure 2: Biomimetic TFBs for nanorobotics: design and cycling [2]

Perspectives

The achieved electrochemical results are among the highest values reported in the literature for such miniaturized energy devices. We believe that our TFB technology [1-3] will contribute to bring new solutions for powering next generation of IoTs, focusing on medical and healthcare applications.

RELATED PUBLICATIONS:
[1] S. Oukassi et al., ACS Appl. Mater. Interfaces, 2019. https://doi.org/10.1021/acsami.8b16364
[2] S. Oukassi et al., PowerMEMS, 2018. https://powermems2018.org/program/PowerMEMS2018_FinalProgram.pdf
[3] S. Oukassi et al., ECS, invited paper, 2018. https://ecs.confex.com/ecs/233/webprogram/Paper108755.html

Advanced Reliability Testing of GaN-on-Si devices

RESEARCH TOPIC:
GaN, pBTI, HEMT, MOSCHEMT, Schottky diodes

AUTHORS:
W. Vandendaele, T. Lorin, R. Gwoziecki, M.-A Jaud, J. Biscarrat, F. Gaillard, (G. Ghibaudo)

ABSTRACT:
LETI's roadmap for GaN-on-Si power transistor and diode devices has reached a high level of maturity which induces an increasing need for reliability testing as well as a deep understanding of the physical mechanisms of the degradations. Gate oxide traps of MOS-channel HEMT (MOSCHEMT) based on Al_2O_3 oxide as well as traps in passivation layers (SiN_x/SiO_2) can be responsible for drift of electrical parameters such as the HEMTs threshold voltage (Vth) and Schottky diodes forward voltage (Vf). This year we have studied ultrafast BTI (bias temperature instabilities) on MOS-channel HEMTs and on Schottky diodes processed on 200 mm GaN-on-Si wafers. This approach enables a deep understanding of the underlying physical mechanisms of instabilities in our devices.

SCIENTIFIC COLLABORATIONS: STM, IRT PowerGaN, IMEP-LAHC

Context and Challenges
GaN-on-Si HEMT technology is undoubtedly considered as the major candidate for medium power applications (650 V rated) due to a combination of high breakdown electric field, electron mobility and electron velocity compared to SiC technologies. Current collapse issue being mainly solved, recent n/pBTI on enhancement-mode pGaN gate HEMTs as well as on the MIS (metal-insulator-semiconductor) gate configuration start showing Vth instabilities, which would severely affect the dynamic performance of the transistors with time. Thus a strong effort has been made to enable the in-depth characterization of Vth/Vf instabilities of our devices through ultrafast Vth MSM (measurement-stress-measurement) sequences, also called ultrafast BTI.

Main Results
Most of the previously pBTI results reported on GaN devices are performed through regular SMUs and allows to study Vth instabilities for long time constants (> 10 ms) leaving in the dark fast Vth instabilities due to unwanted recovery. Therefore we used a fast SMU setup to start recording the Vth shift from the microsecond range (Fig.1) [1].

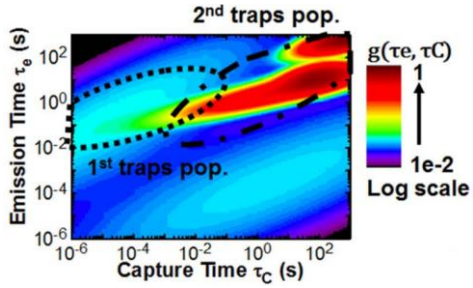


Figure 1: Capture and emission time map giving the traps density g(τc, τe) used to reproduce ultrafast pBTI measurements on MOS-channel HEMTs.

This setup is also used to perform different types of stress (AC/DC) on the gate of the MOS device. By studying large panel of MSM sequences we were able to model the Vth instabilities of MOS-channel HEMT and understand the peculiar degradation kinetic observed experimentally. Moreover, the use of AC stress sequence showed that studying only DC pBTI can lead to an underestimation of the time to failure (TTF) at a given ΔVth criteria (Fig. 2).

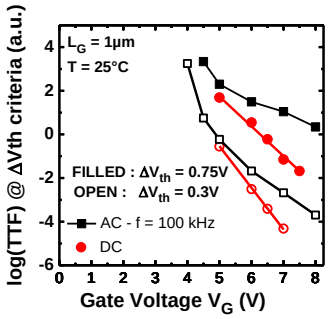


Figure 2: ΔVth time to failure measured under DC and AC gate stress showing TTF underestimation in the case of DC stress.

A similar approach were used on Schottky diodes to determine if a Vf drift can also occurs in these devices [2]. Comparatively to MOS devices, the Schottky diodes only exhibits very low Vf drift under a high forward stress associated to electron trapping into the first insulating layer under the anode field plate.

Perspectives
These ultrafast MSM sequences to study BTI in GaN-on-Si devices are a strong asset for technological maturity assessment. Measurements of pBTI are now a part of the standard qualification procedure for GaN devices at LETI. In perspectives, we are planning for additional studies on new dielectrics, integration and devices design thanks to this advanced reliability testing toolkit.

RELATED PUBLICATIONS:
[1] W. Vandendaele *et al.*, IEEE 56th IRPS conference, 2018. https://doi.org/10.1109/IRPS.2018.8353580
[2] T. Lorin *et al.*, Microelectronics Reliability, 2018. http://dx.doi.org/10.1016/j.microrel.2018.07.103

Characterization and Optimization of III-N Materials for Power Electronics Applications

RESEARCH TOPIC:

High growth rate GaN for reduced fabrication time, and advanced characterization of quaternary alloys.

AUTHORS:

M. Charles, E. Nolot, Y. Mazel, J-P. Barnes, R. Bouveyron, M. Mrad, Y.Baines, A. Bavard, (A.Tempez, S. Legendre)

ABSTRACT:

LETI's work on power electronics using GaN on silicon substrates involves optimization of many different elements in order to improve performance. Although part of this work is directly linked to electrical performance, reduction of fabrication time and advanced characterization are also important as part of the project. In this last year, we have shown that high growth rate GaN has no significant impact on crystalline quality or surface morphology. It also has the benefit of high carbon incorporation, which reduces vertical leakage current, an important device criterion.
In a different study, we have shown that a new fast depth-profiling tool (PP-TOFMS) can provide accurate measurements of difficult to characterize quaternary InGaAlN layers.

SCIENTIFIC COLLABORATIONS: HORIBA FRANCE

Context and Challenges

The epitaxial growth of GaN on silicon involves many different buffer layers, and the whole process takes several hours. One way to reduce this is by increasing growth rates while maintaining the morphological and electrical properties required. This has been applied to the main GaN layer, which is typically 2 µm thick, and so can give the biggest gains.
In parallel, we have worked with advanced "quaternary" layers of InGaAlN alloys, to give very low sheet resistance in the 2 dimensional electron gas (2DEG) formed at the interface between these layers and the GaN channel. The quaternary layers often have unwanted gallium included, so fast and accurate characterization is very important.

Main Results

We have increased the growth rate of GaN layers from typical values around 2 µm/hr up to nearly 15 µm/hr. This had little impact on the surface morphology (Fig.1) and showed only a slight increase in the dislocation density.

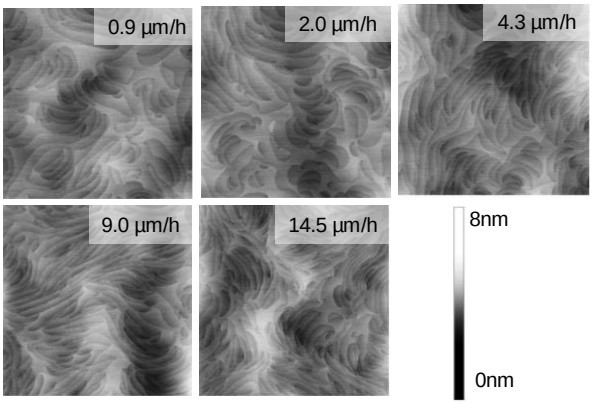


Figure 1: 5 x 5 µm^2 AFM images of GaN surface with growth rate from 0.9 µm/hr to 14.5 µm/hr

A beneficial effect of higher growth rates was greater carbon incorporation, which reduces vertical leakage current, and increases breakdown voltage of these structures. We have thus shown that with our growth conditions we can significantly increase growth rates and even improve the electrical properties of the films at the same time.

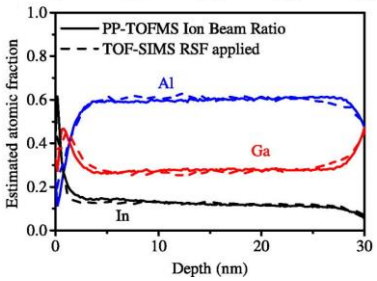


Figure 2: Comparison of atomic fraction depth profiles of In, Al and Ga by PP-TOFMS and TOF-SIMS.

Characterisation of quaternary layers was performed with the new and fast technique of plasma profiling-time of flight mass spectrometry (PP-TOFMS) and compared with the more expensive, slower and well-known technique of time of flight secondary ion mass spectrometry (TOF-SIMS). This showed excellent matching once relative sensitivity factors were applied (Fig.2). This shows that this technique will be an excellent tool for quickly and cheaply characterising these layers.

Perspectives

We have worked to understand the effects of increasing GaN growth rates, to reduce fabrication time, and we find that we even improve the electrical properties. Our new characterisation technique of PP-TOFMS has shown itself to be well matched to TOF-SIMS measurements, and thus is a fast, convenient and accurate way to characterise layers, in particular quaternary layers which are difficult to analyse with other techniques.

RELATED PUBLICATIONS:

[1] M. Charles *et al.*, Journal of Crystal Growth, 2018 https://doi.org/10.1016/j.jcrysgro.2017.11.004
[2] Y. Mazel *et al.*, Journal of Vacuum Science and Technology B, 2018 http://dx.doi.org/10.1116/1.5019635

New Thin Film Materials for Microbatteries

RESEARCH TOPIC:
Lithium(-ion) batteries, microbatteries, thin film, bismuth, $LiMn_2O_4$

AUTHORS:
F. Le Cras, (B. Pecquenard, S. Cotte, N. Sharma, D. Goonetilleke, J. Galipaud)

ABSTRACT:
Thin film electrode materials for all-solid-state lithium(-ion) microbatteries were synthesized by magnetron sputtering as elemental bricks for the make-up of 3 V power supplies. $Fe_2(MoO_4)_3$ intercalation material with the NaSICon structure was investigated as a cathode, whereas Bi and Li_xBi alloys were studied as anodes for Li-ion systems using a $LiCoO_2$ cathodes. The introduction of Bi in all-solid-state cells required an optimization of the deposition process and a better understanding of the mechanisms at stake during the charge/discharge of the cell. The electrochemical performance of the Bi electrode (capacity, cycle life) is finally in accordance with the specifications.

SCIENTIFIC COLLABORATIONS: ICMCB, University of South Wales (Sidney), Australian Synchrotron (Melbourne)

Context and Challenges

With the aim of manufacturing specific microbatteries providing a flat 3 V discharge curve, two types of thin film electrode materials prepared by RF magnetron sputtering have been developed: NaSICon-type $Fe_2(MoO_4)_3$ cathodes [1] and Li_xBi anodes [2] so that these ones can be associated respectively with a Li anode and a $LiCoO_2$ cathode. Whereas the issues related to the synthesis of the iron molybdate were anticipated, particular phenomena were highlighted during the preparation and the operation of Bi thin films.

Main Results

Between these two possible designs, the Li-ion Bi/LiPON/$LiCoO_2$ system has been the preferred option since the $LiCoO_2$ cathode is a high performance standard and is already routinely manufactured in-house. The high sputtering yield of Bi and its low melting temperature required an optimization of the sputtering conditions in order to monitor the roughness and the thickness of the film. The electrochemical alloying/dealloying reaction with lithium occurs in two steps at the appropriate voltage ~ 0.8 V/Li^+/Li (Fig.1) and leads to a high volumetric capacity. The reversibility of the reaction appears quite satisfactory, but the likely formation of nanopores during the dealloying step (suggested by RBS and EIS measurements) leads to a progressive increase of the polarization. Besides, *operando* synchrotron XRD measurements (Fig. 2) have also revealed the formation of an intermediate metastable phase (Li_2Bi).

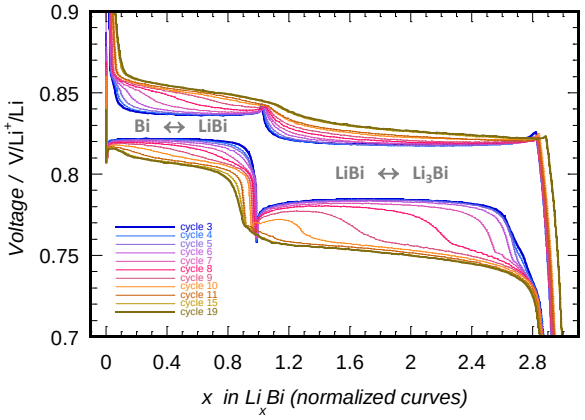


Figure 1: Evolution of the Li_xBi voltage curve upon cycling at constant current revealing the emergence of a porous structure.

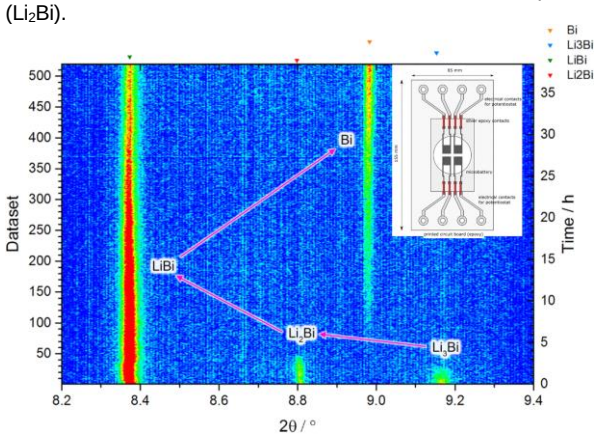
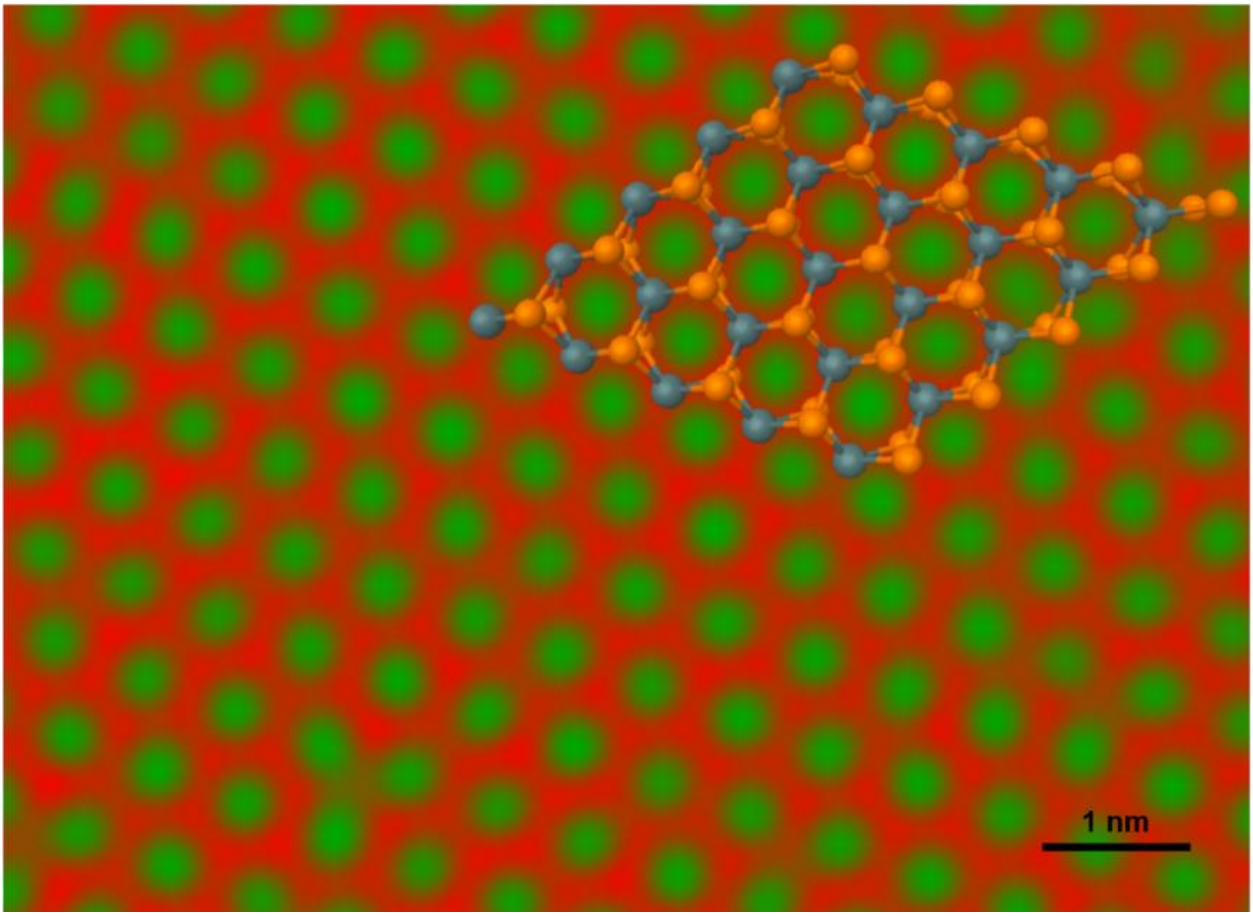


Figure 2: Operando synchrotron X-ray diffraction experiment on a Li_xBi thin electrode revealing the formation of the Li_2Bi metastable phase. Insert: set-up for microbattery characterization.

Perspectives

The introduction of the Bi electrode has led to the study of parent materials (Bi-Sb alloys, Bi_3Ni intermetallics) and the achievement of $LiCoO_2$/LiPON/(Bi,Sb) lithium-ion microbatteries at LETI. The material bricks developed here can be now integrated in different Li-ion systems and/or customized to meet other particular requirements from our partners.

RELATED PUBLICATIONS:
[1] S. Cotte *et al.*, J. Alloys Comp., 2018. https://doi.org/10.1016/j.jallcom.2017.11.231
[2] D. Goonetilleke *et al.*, Frontiers Energy Res., 2018. https://doi.org/10.3389/fenrg.2018.00064


1 nm

06 EMERGING MATERIALS & PROCESSES

- **Impact of Self-Emitted Acoustic Waves on the Fracture Step of Smart Cut™ Technology**
- **Selective Epitaxy of SiGe and Ge in Nanometer-Size Cavities and Holes**
- **Van Der Waals-Layered Ge-Sb-Te Materials for Innovative Phase-Change Memories and Novel Applications**
- **Optimization of GeSn and SiGeSn Epitaxy for Use in Electronics and Photonics Devices**
- **Development of a CMOS-Compatible Contact Module for GeSn**
- **Innovative Magnetic Nanostructures : Process and Characterization**
- **Chemical Sensitive Layers Deposited by CVD for Hydrocarbon Gas Sensors**

Impact of Self-Emitted Acoustic Waves on the Fracture Step of Smart Cut™ Technology

RESEARCH TOPIC:
Layer transfer, Smart Cut™, SOI, Fracture mechanism, Acoustic waves.

AUTHORS:
F. Mazen, (D. Massy), A. Petit, S. Pokam, F. Madeira, P. Acosta, S. Tardif, F. Rieutord, (D. Landru)

ABSTRACT:
Advanced Silicon On Insulator (SOI) substrates require precise control of Si film thickness at local (µm) and wafer (mm) scales. The Smart Cut™ technology enables such control. As a key step of this technology, the fracture mechanisms need to be fully understood. Thanks to dedicated experiments, we have observed a possible interaction between the propagating crack and its self-emitted acoustic wave. This Interaction leads to wafer scale thickness non-uniformity on fractured surfaces and formation of a periodic pattern made of roughness modulations.

SCIENTIFIC COLLABORATIONS: CEA-INAC, SOITEC.

Context and Challenges
Emerging microelectronic applications such as Internet-Of-Things (IOT) or mixed signal processing utilize fully depleted MOSFETs built on SOI wafers (FDSOI). Smart Cut™ technology is the only industrial way that allows the transfer of the extremely thin Si layer (5 - 10 nm range) required for FDSOI based devices. However, since the threshold voltage of FDSOI transistors depends on the thickness of the top silicon layer, it has to be controlled within an extremely tight tolerance (i.e. ± 5 Å) over the whole surface of a 300 mm wafer. These drastic requirements for the most advanced SOI substrates calls for a multiscale understanding and control of the fracture step, which may impact the top silicon surface morphology of SOI wafers made by Smart Cut™ technology.

Main Results
A fundamental mechanism, which contributes to variations of the top Si layer thickness with spatial frequencies in the mm range, has been recently understood [1, 2].
For that, a dedicated experimental setup was developed to study "in situ" the fracture step (fig 1). It allows to measure the propagating crack speed (in the km / s range) via IR transmission and, simultaneously, to record the related acoustic emission via piezoelectric sensors.

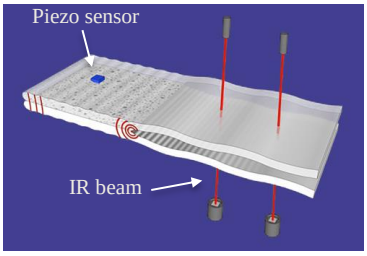


Figure 1: Schematic of the experimental setup for "in situ" study of the propagating crack during the fracture step of Smart Cut™

Using this setup, we observed that the propagating crack interacts with self-emitted acoustic waves and this results in periodic patterns on fractured surfaces. Indeed, measurement of the acoustic emission ahead of the fracture front show the emergence of a dominant acoustic frequency related to the crack velocity. The shear stress field of these waves leads to crack path deviations at a large scale (mm range) and generates periodic patterns made of roughness modulations as shown on fig 2. A physical mechanism explaining the pattern formation, in good agreement with experimental results, was established.

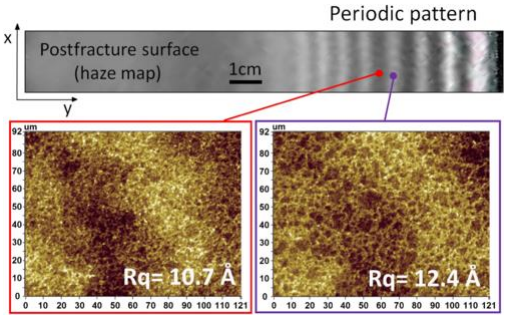


Figure 2: Haze map of the periodic pattern observed on a post-fracture surface (top) and optical interferometer measurements at the bright and dark fringes of the pattern (bottom)

Perspectives
These results strengthen our knowledge of the basic mechanisms involved in the Smart Cut™ technology and will help obtain new insights to further improve SOI wafers characteristics. Moreover, while motivated by SOI applications this study provides new ways to interpret the formation of periodic surface marks on fractured surfaces for a broader class of materials.

RELATED PUBLICATIONS:
[1] D. Massy et al., Physical Reviews Letters, 2018, https://journals.aps.org/prl/abstract/10.1103/PhysRevLett.121.195501
[2] O. Kononchuk et al., ECS meeting, 2018, http://ma.ecsdl.org/content/MA2018-02/35/1175.abstract

Selective Epitaxy of SiGe and Ge in Nanometer-Size Cavities and Holes

RESEARCH TOPIC:
SiGe and Ge Selective Epitaxial Growth, nanometer size templates.

AUTHORS:
M. Mastari, R. Khazaka, Y. Bogumilowicz, M. Charles, M. Argoud, A.M. Papon and J.M. Hartmann

ABSTRACT:
The features of Metal Oxide Semiconductors Field Effect Transistors become smaller and smaller in advanced technology nodes, with (i) a clear switch from planar to 3D devices and (ii) the implementation of new materials (such as SiGe, Ge or III-Vs) in channels or sources / drains. Understanding the Selective Epitaxial Growth (SEG) of such materials in small areas surrounded by dielectrics and finding innovative ways of dealing with lattice parameter / polarity differences is then of paramount importance. We have thus explored the SEG of SiGe in nanometer-size openings (Nano-Hetero-Epitaxy) and of Ge in nanometer-size tunnels (Template Assisted Selective Epitaxy), to gain a better handle on the impact of size, densities of openings or crystallographic orientation on SEG.

INDUSTRIAL COLLABORATION: SOITEC (Nano-Hetero-Epitaxy)

Context and Challenges
Selective epitaxy of group-IV semiconductors is one of the backbones of the Si microelectronics industry. As dimensions become smaller and smaller and the materials used more and more exotic, the use of new epitaxy concepts such as Template Assisted Selective Epitaxy (TASE) or Nano-Hetero-Epitaxy (NHE) in nanometer-size templates becomes attractive. TASE can for instance be used to accommodate the lattice mismatch between Ge or GaAs (5.658 Å or 5.653 Å) and Si (5.431 Å) through the elimination of the threading arms of misfit dislocations in the SiO_2 walls surrounding the tunnels (with Si seeds at their end) being filled (Fig. 1 (top)). Meanwhile, NHE can be used to obtain relatively smooth, nearly fully relaxed 2D SiGe films (Fig. 1 (bottom)).

Main Results
We have evaluated in Ref. [1-2] the impact of using Silicon-On-Insulator substrates as templates for the formation of thin, wide or narrow cavities surrounded by SiO_2 (after the etching of Si thanks to gaseous HCl). A clear impact of the crystallographic direction of the Si seed on extended defects was evidenced, with <100> directions being better than <110> directions. In the end, we succeeded in growing with TASE several hundreds of nm long Ge nanowires free of defects, as shown by Transmission Electron Microscopy.

The NHE of SiGe 25% layers on top of honeycombed nanometer-size holes obtained thanks to diblock copolymer patterning was investigated in Ref. [3-4]. Through a careful optimization of the surface preparation and the epitaxy itself, we succeeded in obtaining smooth (root mean square surface roughness: 0.4 nm only), fully relaxed SiGe 25% films for thicknesses as low as 200 nm (although extended defects such as twins or stacking faults were still present In the layers).

Perspectives
The TASE approach evaluated for the growth of defect-free Ge ribbons could also be used for the integration of direct bandgap, high electron mobility III-V semiconductors as active materials in nMOS or optoelectronics devices. Meanwhile, NHE is being investigated for the growth of thick Ge films. Other masking materials (such as SiN), other pitches and other patterning strategy are also being evaluated in order to reduce the density of extended defect in merged NHE SiGe films.

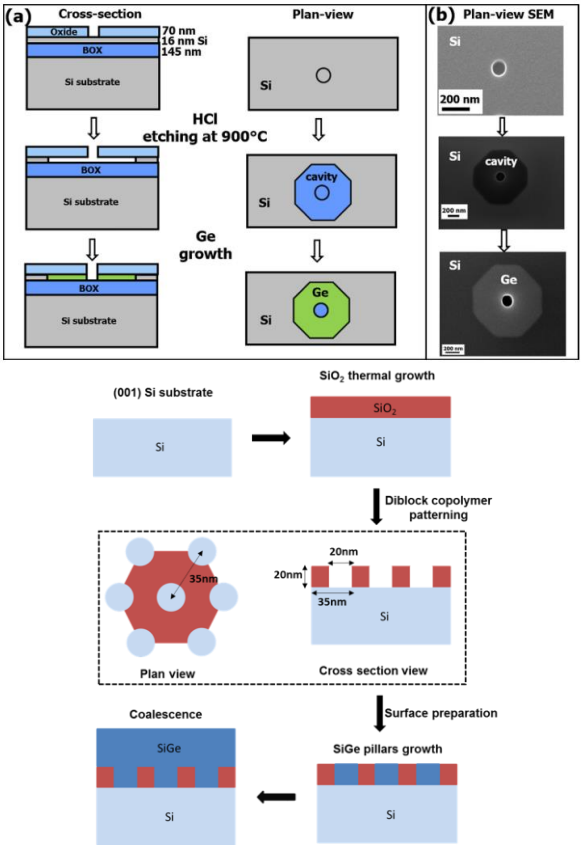


Figure 1: Schematics of (top) TASE and (bottom) NHE approaches used to grow Ge in tunnels and SiGe on top of honey-combed nano-patterns.

RELATED PUBLICATIONS:
[1] R. Khazaka et al., Applied Surface Science, 2018, https://doi.org/10.1016/j.apsusc.2018.03.104
[2] R. Khazaka et al., Applied Physics Letters, 2018 https://doi.org/10.1063/1.5034205
[3] M. Mastari et al., Nanotechnology, 2018, https://doi.org/10.1088/1361-6528/aabdca
[4] M. Mastari et al., ECS Transactions, 2018, https://doi.org/10.1149/08607.0249ecst

Van Der Waals-Layered Ge-Sb-Te Materials for Innovative Phase-Change Memories and Novel Applications

RESEARCH TOPIC:

Non-volatile resistive memories, phase-change memories, chalcogenide, van der Waals growth, GeSbTe

AUTHORS:

P. Noé, N. Bernier, P. Kowalczyk, A. Jannaud, C. Sabbione, M. Bernard, J.-B. Jager, (F. d'Acapito, C. Mocuta, J.-Y. Raty, F. Hippert)

ABSTRACT:

Van der Waals layered (vdW) GeTe/Sb_2Te_3 superlattices (SLs) have demonstrated outstanding performances for use in so-called interfacial Phase-Change Memory (iPCM). Such SLs are made by periodically stacking ultra-thin GeTe and Sb_2Te_3 crystalline layers by means of Van der Waals growth. Our recent experimental studies indicate that the local atomic structure does not correspond to any of the previously proposed structural models. The latter gives a new insight on the complex structure of prototypical GeTe/Sb_2Te_3 SLs demonstrating therefore that an alternative structural model is required to explain the nature of the resistive switching mechanism observed in iPCM devices as well as their other unique properties reported so far in literature.

SCIENTIFIC COLLABORATIONS: Université de Liège, CNR-IOM-OGG c/o ESRF, Grenoble-INP/LMGP, SOLEIL

Context and Challenges

Phase-Change Memory (PCM) based on chalcogenide Phase-Change Materials (PCMs) are the most promising candidate among emerging non-volatile memory technologies. PCM provides a variety of promising features such as fast read and write access, excellent scalability potential, and high endurance [1]. PCM is already a product reality in the Storage Class Memory market. However, PCM technology is challenged to meet strict specifications such as low programming current [2]. To overcome this limit, a promising material engineering approach consists in using a chalcogenide superlattice (SL) in "interfacial Phase-Change Memory" (iPCM) devices in replacement of the conventional bulk GeSbTe alloys of PCM. iPCM cell exhibits significantly lower programming energy, higher endurance and a shorter commutation time than a PCM cell using a GST alloy with the average composition of the SL. iPCM opens numerous opportunities for multi-level storage, hybrid devices combining resistive and magnetic memories, logic gate devices and also devices for THz pulse detection. Incorporation of SLs in iPCM devices by using ULSI microelectronics technology has been demonstrated for large density memory arrays. The origin of these new and improved performances are still unknown and the switching mechanism not yet elucidated is currently highly debated.

Main Results

The SL is designed as a periodic stacking of nm-thick GeTe and Van der Waals (vdW) Sb_2Te_3 crystalline layers grown by means of Van der Waals epitaxy (Fig. 1).

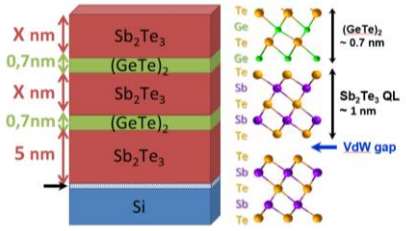


Figure 1: (left) Schematic drawing of the $[(GeTe)_2/(Sb_2Te_3)_m]_p$ periodic stacking deposited for SLs of iPCM devices with thickness and number of the Sb_2Te_3 blocks separated by VdW gaps (1 block= 1 Te/Sb/Te/Sb/Te Sb_2Te_3 quintuple layer (QL) of 1 nm thick). A 5 nm Sb_2Te_3 seed layer is used to initiate VdW growth of the SL. (right) The atomic structures of a Sb_2Te_3 QL and a $(GeTe)_2$ blocks with corresponding thicknesses are also shown.

In iPCM devices, SLs are obtained by Physical Vapor Deposition (PVD) magnetron sputtering in order to produce a SL oriented with the [001] axis (hexagonal indexation). The GeTe layer thickness is most often equal to 0.7 nm which corresponds to the thickness of a $(GeTe)_2$ block (2 Ge and 2 Te planes) in the bulk rhombohedral GeTe phase. SLs can be labelled $[(GeTe)_2/(Sb_2Te_3)_m]_p$ with p the number of periods and m corresponding to the number of Sb_2Te_3 block of 1 nm (1 QL) (Fig. 1).
All models in the literature assume the existence of GeTe layers surrounded by Sb_2Te_3 QLs in the SL. However, our advanced XRD and HAADF-STEM analysis of the optimized and stoichiometric SLs rule out the most used structural models to explain the electrical contrast and the resistive switching of such SLs when incorporated in interfacial Phase-Change Memory devices [3].

Indeed, thanks to development of a damage free TEM sample preparation method for SLs, advanced electron microscopy imaging investigations revealed that GeTe and Sb_2Te_3 layers intermix during the SL deposition and form Ge-Sb-Te blocks containing Ge-rich and Sb-rich Ge/Sb planes (Fig. 2).

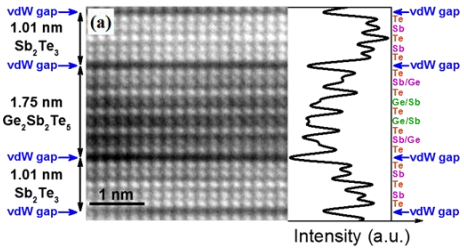


Figure 2: High resolution HAADF-STEM image of a stoichiometric $[(GeTe)_2/(Sb_2Te_3)_4]_{24}$ SL. Curves on the right of each image are vertical linescans integrated over the image width. VdW gaps are indicated with blue arrows. Atomic columns containing heavy atoms (Te or Sb) appear significantly brighter. 2 Sb_2Te_3 QLs and 1 $Ge_2Sb_2Te_5$ block (9 planes) separated by vdW gaps are identified.

Perspectives

The intermixing revealed in our industrial and state-of-the-art stoichiometric GeTe/Sb_2Te_3 SLs must be considered in models aiming at explaining the origin of electrical contrast in iPCM devices. Such an understanding is mandatory to permit iPCM technology to emerge in the future on the non-volatile memory market as well as enabling new applications in spintronic or THz fields.

RELATED PUBLICATIONS:

[1] P. Noé and F. Hippert, *Phase Change Memory*, Springer, Cham, pp. 125–179 (2018). https://doi.org/10.1007/978-3-319-69053-7_6
[2] P. Noé, et al *Semicond. Sci. Technol.* **33**, (2018).https://doi.org/10.1088/1361-6641/aa7c25
[3] P. Kowalczyk *et al.*, *Small* **14**, 1704514 (2018). https://doi.org/10.1002/smll.201704514

Optimization of GeSn and SiGeSn Epitaxy for Use in Electronics and Photonics Devices

RESEARCH TOPIC:
GeSn and SiGeSn growth kinetics, photonics, mid infra-red lasers and photo-detectors

AUTHORS:
R. Khazaka, J. Aubin, E. Nolot and J.M. Hartmann

ABSTRACT:
Si, Ge and Sn elements belong to column IV of Mendeleev's periodic table. They crystallize in a diamond structure, with a lattice parameter for Sn (6.49 Å) which is much higher than that of Si (5.43 Å) or Ge (5.66 Å). Suspended GeSn micro-disks grown on Ge-buffered Si substrates were shown in 2015 to be direct bandgap semiconductors that lased up to reasonable temperatures, sparkling a huge interest in the scientific community for use in devices such as lasers, photodetectors or field effect transistors. Since 2015, we have explored the growth of thin and thick GeSn layers, SiGeSn/GeSn double heterostructures and so on. We will show in the following some of the salient features of the very low temperature epitaxial growth of GeSn and SiGeSn, with perspective on their applications.

Context and Challenges
GeSn-based alloys are promising as the active media of various devices such as mid infra-red lasers and photodetectors, tunnel and metal oxide semiconductor field effect transistors and so on. Strain and chemical content have a huge impact on the bandgap, which can be direct when the tin content is high enough, i.e. above 8%, and the strain in GeSn layers (grown on Ge virtual substrates) nil or tensile.
The growth of Sn containing alloys is far from being trivial, however. Indeed, the solid solubility of Sn in Ge is low. Unless very low growth temperatures and fast growth rates are used, Sn precipitation and surface segregation will destroy the epitaxial quality.
We have thus explored the very low temperature growth of GeSn and SiGeSn in our epitaxy tool and quantified the impact digermane (Ge_2H_6), tin tetrachloride ($SnCl_4$) and disilane (Si_2H_6) have, together with temperature and pressure, on (i) the incorporation of Sn and Si inside the Ge lattice, (ii) the growth rate and (iii) the structural quality of the resulting layers.

Main Results
In Ref. [1], we have quantified the impact temperature had, for given Ge_2H_6 and $SnCl_4$ flows, on the GeSn growth kinetics. We observed a moderate increase of the growth rate and a drastic decrease of the Sn content (from 15% down to 6%) as the temperature increased from 300°C up to 350°C (see Fig. 1a). We also showed that, at a given temperature, the GeSn growth rate increased linearly and the Sn content sub-linearly with the $SnCl_4$ flow. Those findings were confirmed in ref. [2], where the impact of growth pressure and hydrochloric acid flow on the GeSn growth kinetics was also explored. Because of the chlorinated Sn precursor used, the growth of GeSn was shown to be selective against SiO_2 and SiN, which will be useful in future integrations. We also proposed in Ref. [3] an original protocol combining X-Ray Diffraction and X-Ray Fluorescence to determine thickness and chemical contents in SiGeSn layers. We showed that the addition of Si_2H_6 to the gaseous mixture resulted not only in the incorporation of Si, but also in an unforeseen increase of the Sn content (see Fig. 1b). Finally, we quantified the impact temperature and disilane flow had on the SiGeSn growth kinetics.

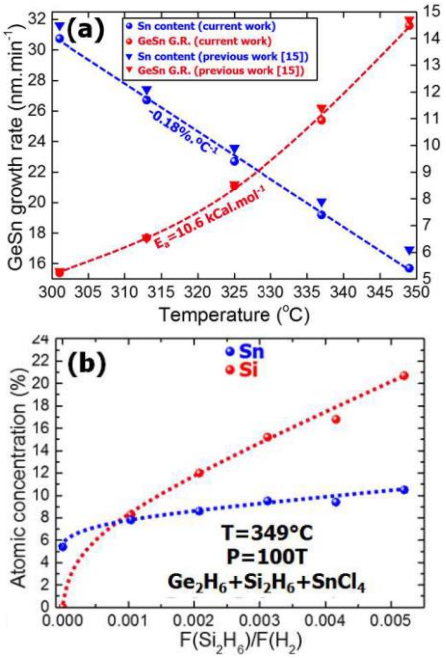


Figure 1: (a) Evolution of the GeSn growth rate and Sn content with the growth temperature for given precursor flows and (b) evolution of the Si and Sn content with the Si_2H_6 flow at a given T ([2]).

Perspectives
Starting from thick GeSn, step-graded structures (with SiGeSn electronics barriers below and above) on top of Ge virtual substrates, we recently succeeded in obtaining the current world record in terms of lasing temperature and wavelength, i.e. 230K and 3.1 µm [4]. We are currently evaluating the properties of GeSn / SiGeSn photonic crystals, photodetectors and suspended micro-bridges, the aim being for instance to have low threshold, electrically pumped mid infra-red lasers operating at room temperature.

RELATED PUBLICATIONS:
[1] J. Aubin and J.M. Hartmann, Journal of Crystal Growth (2018) https://doi.org/10.1016/j.jcrysgro.2017.10.030
[2] R. Khazaka *et al.*, ECS Transactions (2018) https://doi.org/10.1149/08607.0207ecst
[3] R. Khazaka *et al.*, Semiconductor Science and Technology, (2018) https://doi.org/10.1088/1361-6641/aaea32
[4] Q.M. Thai *et al.*, Optics Express (2018) https://doi.org/10.1364/OE.26.032500

Development of a CMOS-Compatible Contact Module for GeSn

RESEARCH TOPIC:

GeSn, Contacts, Surface preparation, Metallization, Ni(Pt)

AUTHORS:

A. Quintero, P. E. Raynal, J. M. Hartmann, V. Loup, P. Gergaud, V. Reboud, Ph. Rodriguez (E. Cassan, L. Vallier)

ABSTRACT:

GeSn-based alloys are promising for the monolithic integration of light sources in mid infrared CMOS-compatible Si photonic circuitry. Semiconductor optoelectronic devices need efficient metallic contacts to receive and deliver power and signal. The development of a CMOS-compatible contact module for GeSn materials has therefore been initiated. In combination with dedicated surface preparation schemes, Ni-based stanogermanides (Ni-GeSn) yielded low specific contact (R_c) and sheet (R_{sh}) resistances on GeSn surfaces to contact efficiently GeSn-based photonic or electronic devices. It was also demonstrated that the addition of Pt positively influenced the contact properties.

SCIENTIFIC COLLABORATIONS: C2N/CNRS/Univ. Paris-Sud, LTM

Context and Challenges

GeSn, a group IV binary alloy, is currently of high interest. Its use is envisioned in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and as a direct band-gap material for Si photonics. Low-resistive contacts are key in order to obtain high performance components. A CMOS-compatible contact module has therefore been developed. The surface preparation of GeSn layers together with Ni-GeSn intermetallics were investigated. However, some thermal stability issues were observed. The addition of 10 at.% of Pt was shown to extend the thermal stability and stabilize the intermetallic's properties.

Main Results

A first study coupling wet cleaning and in-situ plasma treatments was conducted for GeSn surface preparation prior to metallization [1]. Then, a comprehensive investigation of the solid-state reaction between a Ni thin film and $Ge_{0.9}Sn_{0.1}$ layers was performed [2]. First, an hexagonal Ni-rich phase (ε-$Ni_5(Ge_{0.9}Sn_{0.1})_3$) was obtained prior to the formation of the mono-stanogermanide phase: Ni(GeSn), as shown in Fig. 1.

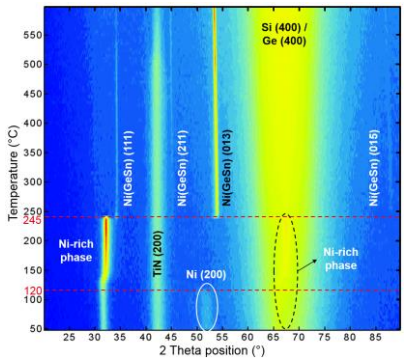


Figure 1: In situ X-ray diffraction measurement of the reaction between Ni and $Ge_{0.9}Sn_{0.1}$ [2].

A low thermal stability of the Ni(GeSn) phase (because of Sn segregation) together with compound agglomeration were evidenced. The addition of 10 at.% of Pt into Ni thin films and its impact on phase sequence, surface morphology and electrical properties were therefore explored [3,4].

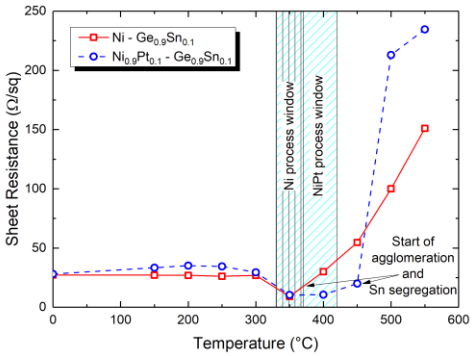


Figure 2: Evolution of the sheet resistance as a function of the annealing temperature for Ni- and NiPt-$Ge_{0.9}Sn_{0.1}$ systems [3].

We showed that Pt had a positive impact on surface morphology and roughness by delaying NiGeSn agglomeration and Sn segregation. The addition of Pt stabilized the electrical properties of the stanogermanide over a wider temperature range, as shown in Fig. 2.

Perspectives

GeSn surface preparation prior to metallization will be fine-tuned thanks to the use of quasi in-situ characterization. Combined with a thorough study of the solid-state reaction of Ni-based metallizations with various Sn content GeSn layers, it should result in the development of a complete CMOS-compatible contact module for GeSn materials. The latter will be used during the elaboration of silicon photonic devices.

RELATED PUBLICATIONS:

[1] P. E. Raynal et al., Microelectronic Engineering 203/204, 2019, 38-43, https://doi.org/10.1016/j.mee.2018.11.005
[2] A. Quintero et al., Journal of Applied Crystallography 51, 2018, 1133-1140, https://doi.org/10.1107/S1600576718008786
[3] A. Quintero et al., Journal of Applied Physics 124, 2018, 085305, https://doi.org/10.1063/1.5040924
[4] A. Quintero et al., ECS Transactions 86, 2018, 299-307, https://doi.org/ 10.1149/08607.0299ecst

Innovative Magnetic Nanostructures: Process and Characterization

RESEARCH TOPIC:
Nanolaminate, nanoparticles, magnetic properties

AUTHORS:
R.Hida, (C.V.Falub), S.Perraudeau, C.Morin, S.Favier, Y.Mazel, J-P. Michel, B. Morcos, P.H. Haumesser, (C.C. Santini)

ABSTRACT:
We report the elaboration of innovative magnetic nanostructures. First a method to produce nanostructured soft magnetic multilayers is presented, the properties of which can be easily tuned by choosing the ratio of the individual nanolayers. In this way it is possible to combine soft magnetic materials with complementary properties, e.g. high saturation magnetization, low coercivity, high specific resistivity and low magnetostriction. In addition, a new synthetic procedure is introduced to produce Co nanoparticles with controlled size and structure.

SCIENTIFIC COLLABORATIONS: Evatec, Nanochemistry Platform CEA-CPE Lyon

Context and Challenges
Nanocrystalline magnetic materials because of their interesting functional properties such as their ductility, high wear resistance, mechanical strength and magnetic properties have attracted significant attention from many researchers. Such materials find potential applications in diverse areas like medical, aerospace and microelectronic technologies as: sensors, thermal and chemical resistant materials, radio-frequency thin film inductors, micro-electromechanical systems (MEMS), micro inductors, computer read/write heads and memory devices. The main challenges are the precise control of size, composition and morphology.

Main Results
We explored the potential for tailoring novel materials with enhanced magnetic properties by combining the characteristics of individual ferromagnetic constituents [1,2]. The thickness of these individual sputtered nanolayers were adjusted by changing the process conditions and hardware configuration. The thin film materials deposited in this manner exhibited a nanolayered structure as shown by XRD and TEM analyses (Fig 1). We showed that the electrical (resistivity) and magnetic properties (e.g. M_s, H_k, H_c,magnetostriction) could be adjusted easily by changing the proportion of each individual magnetic nanolayer. This method turned out to be an excellent mode to engineer new composite ferromagnetic materials with tunable functional properties.

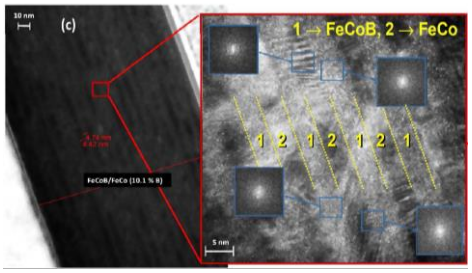


Figure 1: TEM cross-section micrographs and diffraction patterns of the FeCoB/FeCo multilayers with B content of 10.1%.

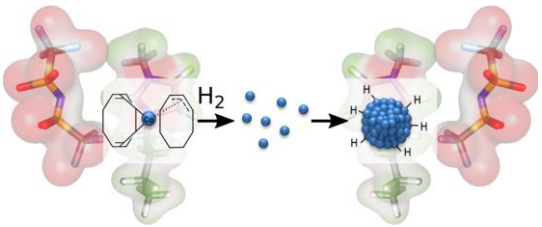


Figure 2: Principle of Co-NP synthesis in ionic liquids

A chemical process to elaborate cobalt magnetic nanoparticles (NPs) was also considered, using ionic liquids (molten salts at room temperature) as the reaction media [3]. Imidazolium-based ionic liquids (ILs) were successfully used to elaborate magnetically responsive suspensions of quite monodisperse Co-NPs with diameters below 5 nm. The as synthesized Co-NPs adopted the non-compact and metastable structure of ϵ-Co that progressively evolved at room temperature toward the stable hexagonal close-packed allotrope of Co. Accordingly, magnetization curves were consistent with zero-valent Co. As expected, the Co-NPs were super-paramagnetic at room temperature. The Co-NPs produced in an IL with a large cation exhibited a very high anisotropy, attributed to an enhanced dipolar coupling of the NPs.

Perspectives
The multilayer sputtering method can be applied to more than two materials at the same time, and other material combinations, including magnetic/nonmagnetic ones, potentially paving the way for integrated thin film magnetic cores with dramatically improved properties.
In addition to their promising magnetic properties, Co-NPs were shown to possess surface hydrides. This paves the way toward the synthesis for Co-based bimetallic NPs (e.g. core shell NPs with a Co core).

ELATED PUBLICATIONS:
[1] R.Hida and al, Journal of Magnetism and Magnetic Materials, 2018, http://dx.doi.org/10.1016/j.jmmm.2018.01.022
[2] C.V.Falub and al, AIP Advances, 2018, http://dx.doi.org/10.1063/1.4993688
[3] B.Morcos and al, American Chemical Society, 2018, http://dx.doi.org/10.1021/acs.langmuir.8b00271

Chemical Sensitive Layers Deposited by CVD for Hydrocarbon Gas Sensors

RESEARCH TOPIC:
Polymer and organosilicate thin films, iCVD, PECVD, FACVD, gas sensors

AUTHORS:
V. Jousseaume, J. El Sabahy, F. Ricoul, C. Ladner, E. Ollier, (J. Faguet)

ABSTRACT:
The fabrication of gravimetric gas sensors based on nano electro mechanical systems requires the use of a chemical sensitive layer that is uniformly deposited by a solvent-free deposition technique. In this work, different approaches were used to develop polymer and organosilicate thin films suitable for the detection of light alkanes and aromatic volatile organic compounds. We show that organosilicate layers deposited by chemical vapor deposition-based techniques present very high affinity toward hydrocarbon gas. The hydrophobic nature of these materials composed of a Si-O-Si backbone with methyl groups bonded to the silicon results in a very high sensitivity in comparison with other materials.

SCIENTIFIC COLLABORATIONS: TOKYO ELECTRON LIMITED (TEL)

Context and Challenges

The fabrication of gravimetric gas sensors based on nano electro mechanical systems (NEMS) requires the use of a chemical sensitive layer that collects and concentrates the target molecules. To be compatible with an integration on nanometric devices, a thin film of this chemical sensitive layer has to be deposited using a solvent-free deposition technique. In this frame, we have studied the potential of polymer and organosilicate thin films deposited by different chemical vapor deposition (CVD) techniques for alkanes and aromatic volatile organic compounds (VOCs) detection.

Main Results

Functionalized Poly(methacrylates) deposited by initiated CVD (iCVD) were compared to organosilicate thin films deposited by plasma-enhanced chemical vapor deposition (PECVD) or filament-assisted CVD (FACVD). Among all these materials that can simultaneously detect light alkanes and aromatic VOCs, SiOCH thin films appear to be the best candidates (Fig. 1).

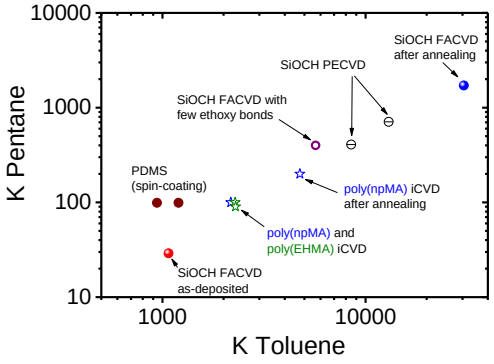


Figure 1: Partition coefficients K (at infinite dilution) for toluene and pentane of polymers and organosilicates deposited by CVD-based techniques. High K value reflects a strong affinity with the gas.

By varying the precursors and the deposition conditions, the chemical composition of SiOCH was tailored in order to optimize their adsorption properties [1]. A tradeoff is necessary on the methyl groups concentration in order to keep high adsorption properties as well as material hydrophobicity. By using filament-assisted CVD, we were able to increase the presence of isolated ethoxy groups that allow a further increase in sensibility in comparison to SiOCH deposited by PECVD [2].

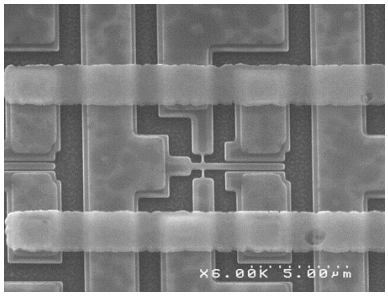


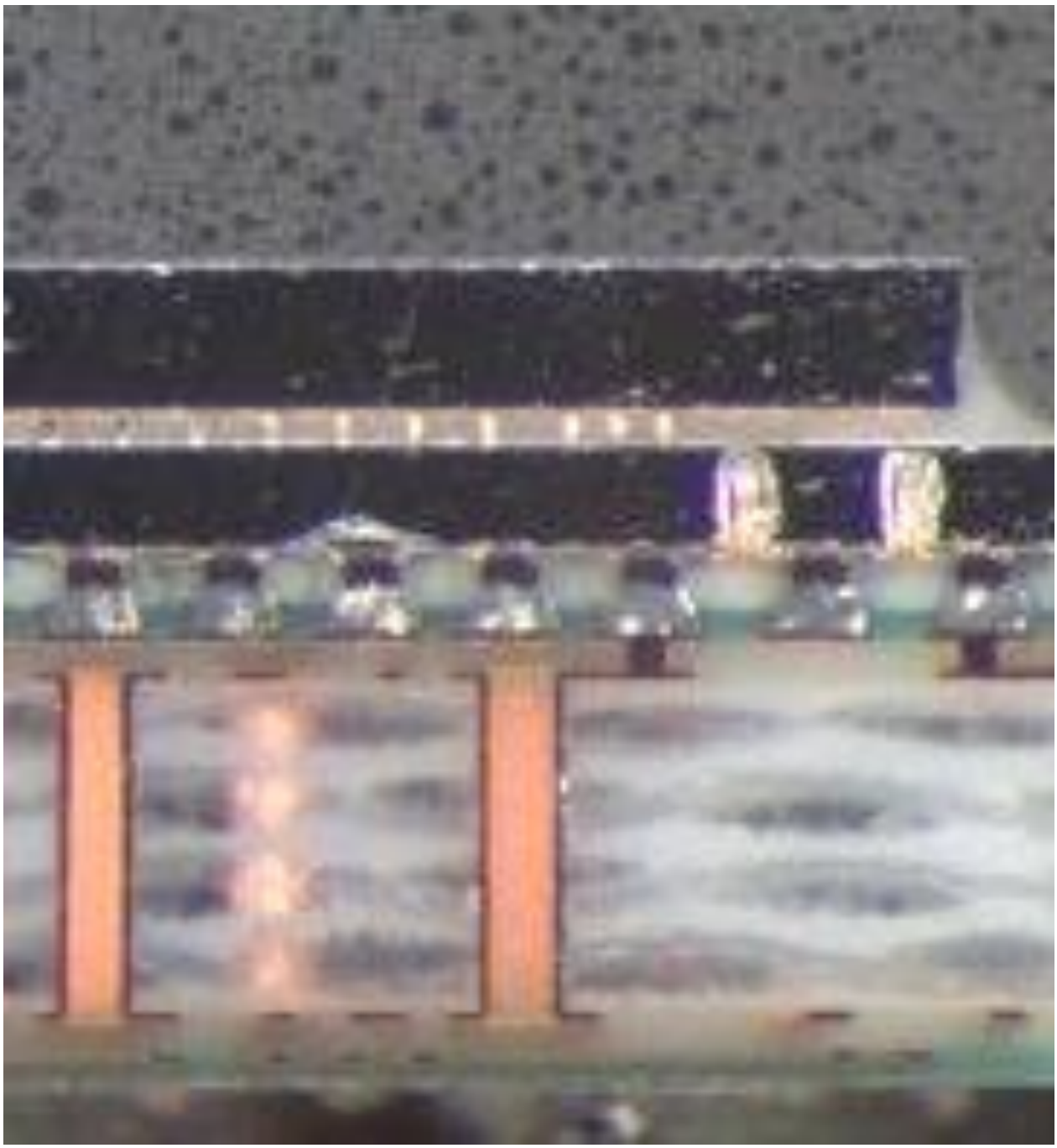
Figure 2: SEM pictures of a NEMS functionalized with a thin SiOCH layer deposited by filament-assisted CVD.

The most promising materials were successfully integrated on NEMS-based gas sensors. Indeed, the CVD techniques used in this work are all compatible with the functionalization of freestanding Si nanocantilevers. The nanometric sensors functionalized with the optimized chemical sensitive layer present a good sensibility for the detection of hydrocarbons and a high level of stability in the range investigated [2].

Perspectives

Current researches are focused on the chemical vapor deposition of new chemical sensitive layers (such as Metal-Organic Frameworks) in order to detect small toxic industrial chemicals. Another research area is the development of porous thin films to detect small molecules in liquid.

RELATED PUBLICATIONS:
[1] J. El Sabahy et al., Sensors and Actuators B 258 (2018) 628-636, http://dx.doi.org/10.1016/j.snb.2017.11.105
[2] V. Jousseaume et al., Sensors and Actuators B 271 (2018) 271-2791, http://dx.doi.org/10.1016/j.snb.2018.05.042



07 3D INTEGRATION & PACKAGING

- **Hybrid Bonding Interconnects for 3D Stacked Image Sensors: Impact of Pitch Shrinkage on Interconnect Robustness**
- **Advanced Solutions for Thermal Management**
- **Backside Protection against Physical Attackson Secure Chips or SiP**

Hybrid Bonding Interconnects for 3D Stacked Image Sensors: Impact of Pitch Shrinkage on Interconnect Robustness

RESEARCH TOPIC:

Hybrid direct bonding, 3D integration, 3D interconnection, wafer to wafer bonding (W2W), CMOS image sensor.

AUTHORS:

L. Arnaud, J. Jourdon, S. Moreau, A. Jouve, F. Fournel, G. Maugen C. Euvrard, Y. Exbrayat, V. Balan, N. Bresson (S. Lhostis), (E. Deloffre), (A. Farcy)

ABSTRACT:

Hybrid bonding is a high density technology for 3D integration. The study of the influence of hybrid bonding pitch shrinkage from 8.8 to 1.44 µm has been performed from process, device performances and robustness perspectives. Electro-optical tests of BackSide Illumination CMOS Image Sensors (BSI CIS) demonstrate no fine pitch hybrid bonding impact on the BSI CIS performance. Aging tests point out no failure related to the hybrid bonding metal pad pitch shrinkage. These results show the robustness of Cu damascene hybrid bonding interconnection down to 1.44 µm pitch.

SCIENTIFIC COLLABORATIONS: IRT3D, POLIS, STMicroelectronics

Context and Challenges

The emergence of 3D stacked BackSide Illumination (BSI) technology makes hybrid bonding process a key solution for CMOS Image Sensors (CIS). A high level of maturity has been previously demonstrated for hybrid bonding pad pitches from 5 to 10 µm justifying the prediction of a significant growth of this technology in the field of CIS for the next years. A low interconnection pitch would enable to increase interconnect density and to reduce the pixel size for applications such as single photon avalanche diodes (SPAD). The impact of reducing hybrid bonding pitch is investigated by comparing bonding quality, electrical and optical performances of 3D stacked CIS with 8.8 to 1.44 µm hybrid bonding pitches.

Main Results

The demonstrators are integrated on 300 mm wafers. A BSI CIS is stacked on a digital CMOS technology node. Wafers are connected thanks to hybrid bonding metal pads (HBM) and hybrid bonding vias (HBV) processed with a Cu damascene architecture. The wafer-to-wafer face-to-face hybrid bonding process is performed on an EVG GEMINI® wafer bonding system followed by a bonding annealing at 400 °C.

Hybrid bonding relies on global flatness and local topography. A controlled planarization process is thus required and a dedicated CMP process has been developed to obtain the required dishing from 1.44 to 8.8 µm pitch on the same wafer. Cu-Cu bonding also relies on thermal expansion of Cu and on atom diffusion at bonding interface. TEM pictures (Fig. 1) evidence a good closing of the Cu-Cu interface whatever the pitch. The robustness of the bonding interface has been qualified with aging tests. Delamination risk is investigated with thermal cycling experiments where the test structures remain fully functional after 500 cycles and do not provide any resistance variation despite a higher stress pointed out by simulation for the smallest pitch [1]. Electromigration failure analysis gives the same mechanism for small and large pitches where lifetime is actually limited by BEOL performance so that the voids are induced in the metal lines below the HBV via [2].

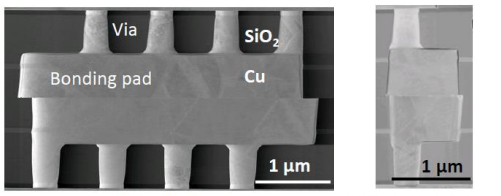


Figure 1: TEM cross sections of face-to-face hybrid bonding interface well bonded for small and large pitch.

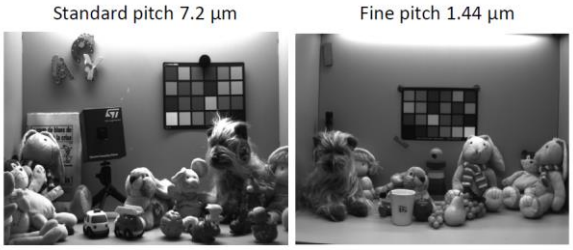


Figure 2: Pictures taken with 3D stacked image sensors with small and large pitch.

Perspectives

The transition of hybrid bonding pitch from 8.8 to 1.44 µm has been made possible thanks to the development of a new surface preparation process enabling flat and required dishing for hybrid direct bonding process. Aging tests point out no failure related to the HBM pitch shrinkage. These results evidence the robustness of Cu damascene hybrid bonding down to 1.44 µm pitch. Next step is to develop a three layer technology for CIS with stacking a pixel wafer, a memory wafer, a logic wafer and improve the device performance.

RELATED PUBLICATIONS:

[1] J. Jourdon et al., IEDM Conference 2018, https://doi.org/10.1109/IEDM.2018.8614570

[2] L. Arnaud et al., IRPS Conference 2018, https://doi.org/10.1109/IRPS.2018.8353591

Advanced Solutions for Thermal Management

RESEARCH TOPIC:
Thermal management, cooling, hot spots, heat spreading, microfluidics

AUTHORS:
P. Coudrain, J.-P. Colonna, Q. Struss, G. Savelli, (L.G. Fréchette), (L.-M. Collin), (J. Barrau)

ABSTRACT:
Circuit environment has evolved to face an ever-increasing thermal challenge, from early design stage down to the final package. Innovative technologies and concepts were explored for efficient thermal management from low to high power electronics, with an emphasis on hot spot management. Passive cooling was treated with high conductivity materials such as pyrolytic graphite or more complex structures such as embedded vapor chambers. Active cooling was achieved with silicon embedded microchannels and complemented with an original approach of self-adaptive fluidic networks to improve cooling efficiency. In both cases, integrations on silicon were demonstrated.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, Université de Sherbrooke (Canada), Universitat de Lleida (Spain)

Context and Challenges
Increase in power densities constitutes a critical challenge for modern ICs as a major part of dissipated power results in heat generation. Temperature rise degrades device performance and reliability whereas hot spot profiles exacerbate intra-chip variability. Addressing thermal challenges from a technological point of view deals with heat extraction and mitigation of hot spots. Modern approaches are entering a fusion era where these solutions are not only taken into account at the design stage but also processed in the fab. Cooling features are integrated close to hot sources with a technological toolbox that spreads from packaging to 3D-integration processes [1].

Main Results
Background studies of heat transfers were carried out at die and package levels on specific test vehicles including 3D ICs. Technological developments were then built up for passive and active cooling. Carbon-based heat spreaders were studied: pyrolytic graphite has exhibited excellent hot spot mitigation capabilities and integration of patterned heat spreaders was demonstrated for 3D hybrid-bonded circuits. A more advanced evolution of heat spreading under development consists in embedding vapor chambers in silicon, at chip or package level. With a principle based on liquid/vapor phase change of a fluid (Fig. 1), this technique exhibits an effective thermal conductivity beyond the one of best conductive materials [2].

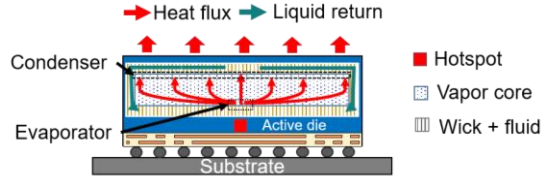


Figure 1: vapor chamber principle: fluid vaporizes at hot spots, goes to vapor core, condensates on colder areas and goes back to hot spots by capillarity through the wick

Active liquid cooling, based on microfluids incorporated in silicon, overcomes the limitations of conventional air cooling in high power systems. Optimizations of the microchannels geometry have been demonstrated for thermal profiles with hot spots [3]. Narrow channels and dense pin fins (Fig. 2) were used near hot spots with wider channels on the background areas, resulting in compact, highly efficient and low thermal resistance cooling solutions. In a more prospective approach, design-independent and self-adaptive fluid networks have been explored in the European STREAMS project, with a capacity to respond to time-dependent thermal loads [4]. This approach is based on networks of microfluidic cells where local flows are self-adapted by microvalves and heat exchange with the fluid is increased by adaptive fins that rise spontaneously with temperature.

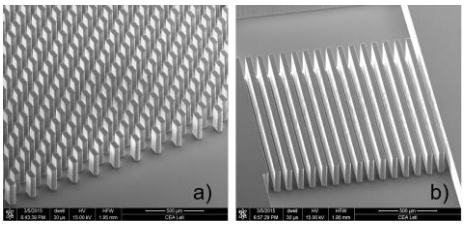


Figure 2: Microfluidic patterns etched in silicon: a) staggered pin fins array c) narrow localized microchannels optimized for hot spot management

Perspectives
Future developments could move towards the add-on integration of these technologies by bonding to give added value to interposers and packages. The technologies developed would provide near-junction cooling systems capable of meeting the thermal challenge of future heterogeneous low to high power systems.

RELATED PUBLICATIONS:
[1] P. Coudrain et al., IEEE Symposium on VLSI Technology, 2018, https://doi.org/10.1109/VLSIT.2018.8510677
[2] Q. Struss et al., International Workshop on Thermal Investigations of ICs and Systems THERMINIC, 2018, https://doi.org/10.1109/THERMINIC.2018.8593326
[3] L.-M. Collin et al., IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, https://doi.org/10.1109/TCPMT.2018.2874241
[4] J. Colonna et al., International Workshop on Thermal Investigations of ICs and Systems THERMINIC, 2018, https://doi.org/10.1109/THERMINIC.2018.8593310

Backside Protection against Physical Attacks on Secure Chips or SiP.

RESEARCH TOPIC:

Cybersecurity, Packaging, Physical Attacks, Shield, System-in-Package (SiP)

AUTHORS:

S. Borel, L. Duperrex, E. Deschaseaux, R. Wacquez, S. Anceau, J. Clédière, A. Merle, B. Charrat

ABSTRACT:

A structure intended to protect Integrated Circuits (ICs) against physical attacks has been designed, developed and evaluated. Located on the backside of a chip, it complements the countermeasures usually available on the front side of secure components. It aims at preventing attacks such as fault injection by laser illumination and can trigger an alert in case of invasive attacks by circuit edit or micro-probing. Our backside shield combines several elements than can be fabricated using packaging technologies in a wafer-level integration scheme, whether at chip or system scale. It opens perspectives for components that are fully secured by the packaging.

Context and Challenges

In our increasingly connected world, electronic devices are meant to manage, store and share more and more sensitive and personal data. Cybersecurity has become a major challenge that requires not only software but also hardware protections to guarantee our security and privacy. Indeed, hackers are in a continuous improvement process. In particular, due to the presence of effective countermeasures on the front side of secure ICs, they have developed techniques to access the active parts of the devices from the backside of the chips. The shield that we designed is meant to prevent them from injecting faults with an infrared laser through the silicon substrate and from digging a cavity in order to probe metal lines and retrieve secret keys or other confidential data.

Main Results

A set of countermeasures has been implemented in a structure that was fabricated using processes based on 3D integration technologies such as deep etching, conformal deposition or film lamination under vacuum. A metallic serpentine embedded in a black (opaque) polymer acquaints the IC with attempted intrusions and is supplemented by weakening structures that cause the mechanical breakage of the chip in case of thinning or digging (Fig. 1).

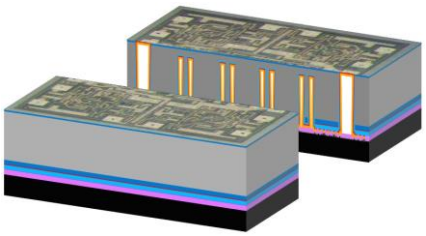


Figure 1: Cross-sectional schematic view of a backside shield with weakening structures and a metal serpentine embedded in polymer.

We successfully designed and manufactured a demonstrator including this backside shield. Some 'state of the art' attacks were then perpetrated to evaluate the effectiveness of our solution. It showed to be resistant to chemical attacks, focused ion beam (FIB) digging and circuit edit, fault injection by laser and micro-milling.

These results at chip level encouraged us to consider extending the concept to a higher scale, namely to a System-in-Package (SiP) with our shield covering the backside of a set of several chips (Fig. 2).

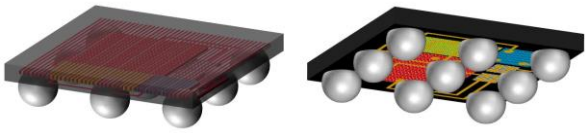


Figure 2: Schematic view of a secure System-in-Package including a collective backside shield embedded in the package.

The assembly, in a single package, of several chips with countermeasures on the front side only, thus leads to a SiP with a two-sided protection. This is of major interest for actors who need to increase the security level of their system still using commercial dies, without designing their own IC.

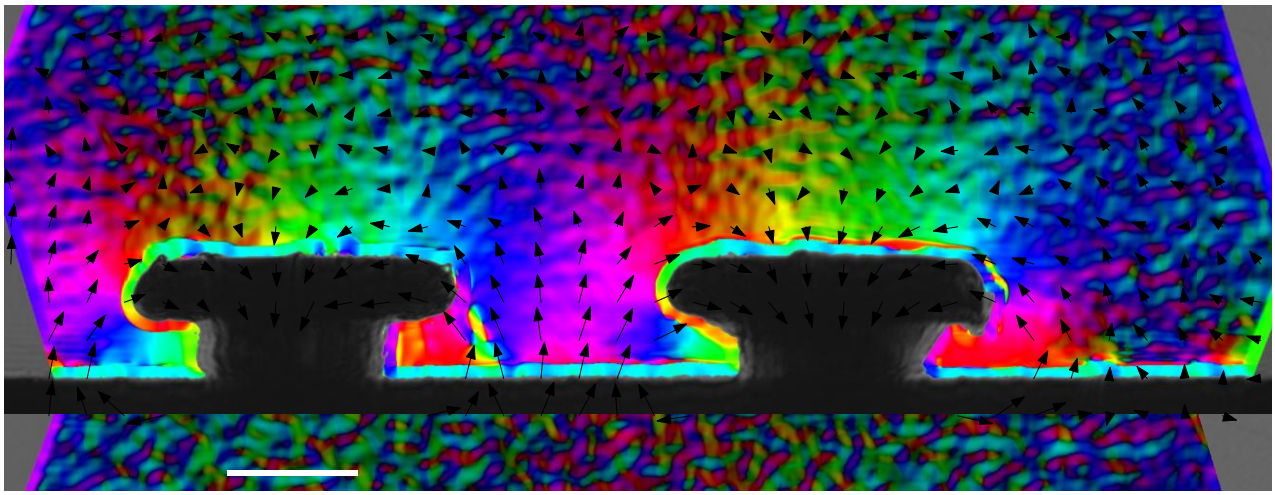
Perspectives

In order to make this technology accessible to more customers, we consider an alternative integration using a silicon interposer, which allows to also protect the front side of chips that are not secured by design, thus obtaining a system *fully secured by the packaging*. In parallel, we plan to extend our offer to customers involved in traditional packaging (chip(s) inside an individual ceramic or metal case) by studying security solutions inside the cavity of the case.

RELATED PUBLICATIONS:

[1] S. Borel et al., IMAPS 13th Device Packaging Conference (DPC), 06-09 / 03 / 2017, Fountain Hills, AZ, USA

[2] S. Borel et al., IEEE 68th Electronic Components and Technology Conference (ECTC), 2018, https://ieeexplore.ieee.org/abstract/document/8429594



08 PHYSICAL-CHEMICAL CHARACTERIZATION & METROLOGY

- **Pushing Electron Holography for Field Mapping at the Ultimate Spatial Resolution and Sensitivity**
- **TOF-SIMS Depth Profiling of Hybrid Organic/Inorganic Devices**
- **Advanced X-Ray Characterisation : Application to Thin Films for Memory Devices**
- **High Spatial Resolution Kelvin Force Microscopy: Application to Nanostructured and Photoactive Materials**
- **Multi-Technique Approaches to 3D Imaging**
- **Correlation of Cathodoluminescence and (S)TEM for Defects Analysis in III-V Material**
- **Probing Critical Buried Interfaces with Hard X-Ray Photoemission**
- **Advanced Microscopic Characterization of the Electronic Properties of 2D Materials**
- **In Depth Analysis of Molecular Cross-Contamination in FOUPs**

Pushing Electron Holography for Field Mapping at the Ultimate Spatial Resolution and Sensitivity

RESEARCH TOPIC:
Field Mapping, Transmission Electron Microscopy

AUTHORS:
David Cooper and Victor Boureau

ABSTRACT:
To meet the demand for field mapping with high sensitivity and spatial resolution, new methods have been developed to improve off-axis electron holography. Off-axis electron holography is a transmission electron microscope based technique which uses electron interference to measure the phase of the electrons and reveal information about the electric, magnetic and strain fields. We have developed and automated methods to control the microscope and to acquire and align large stacks of holograms to improve the signal to noise ratio. Novel hologram reconstruction techniques are used to provide spatial resolutions of 1 nm or better. These methods have been applied to a range of semiconductor materials for CMOS and opto-electronic applications.

SCIENTIFIC COLLABORATIONS: CNRS-CHREA V, INAC

Context and Challenges

Control of the electrostatic and strain fields is an important parameter in the design of semiconductor devices. In order to be able to understand and improve their electrical properties, it is important to be able to quantitatively measure these internal fields with high spatial resolution.

Main Results

Using computer control we are now able to automate the acquisition of large series of electron holograms that are aligned and processed using novel reconstruction methods. This allows quantitative measurement of the electrostatic potentials with 1 nm spatial resolution. Figure 1 shows the experimental and simulated conduction band potentials in a 2.2 nm thick InGaN QW structure that is used for light emission. These methods can also be used to measuring the dopant potentials as well as the magnetic fields in the nano-scaled electronic devices that are currently being developed.

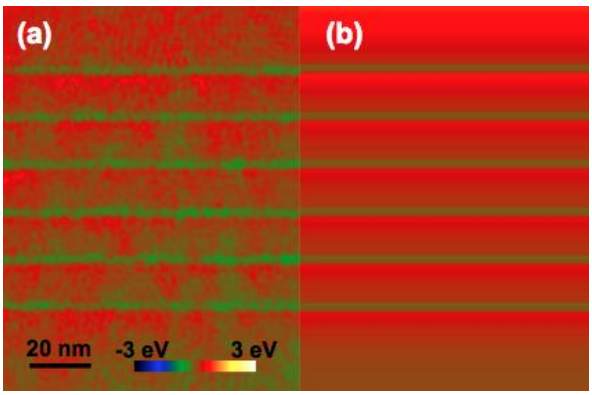


Figure 1: (a) Potential map and (b) simulations of the conduction band in a series of 2.2 nm thick InGaN quantum wells.

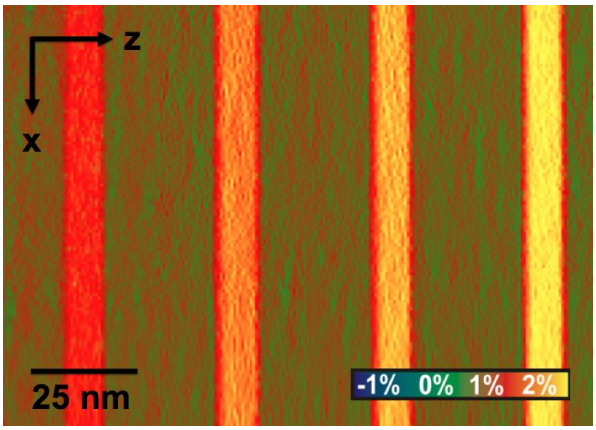


Figure 2: Deformation map of a Si specimen with SiGe layers of different Ge concentrations with 1 nm spatial resolution.

Figure 2 shows a deformation map for the growth direction of a Si/SiGe specimen with different Ge concentrations. As the specimen is in perfect epitaxy the expansion of the lattice parameter relative to the silicon substrate can be measured. The spatial resolution and sensitivity allows the strain fields to quantitatively be measured in the smallest device specimens.

Perspectives

The developments of electron holography now allows quantitative measurements of the electric, magnetic and strain fields at the required spatial resolutions for semiconductor research. They are today being used for a range of applications such as the development of opto-electronic devices where the complex interplay between dopants, strain and piezo-electric fields determines their optical properties, for the development of magnetic memories, as well as for conventional CMOS characterisation.

RELATED PUBLICATIONS:
[1] B. Haas et al, Ultramicroscopy 198, 58-72 (2019) http://dx.doi.org/10.1016/j.ultramic.2018.12.003
[2] V. Boureau et al, Ultramicroscopy 193, 52-63 (2018) https://doi.org/10.1016/j.ultramic.2018.06.004

TOF-SIMS Depth Profiling of Hybrid Organic/Inorganic Devices

RESEARCH TOPIC:
Nanocharacterisation, depth profiling, OLED

AUTHORS:
J. P. Barnes, T. Terlier, G. Beainy, T. Maindron, (F. Bassani, D. Leonard)

ABSTRACT:
In order to address new materials and devices with time-of-flight secondary ion mass spectrometry (TOF-SIMS) the use of new ion beams and analysis protocols are required. Here we present the developments performed to increase the depth resolution for the depth profiling of thin III-V multilayer structures and to enable the characterisation of ageing in organic electronic devices such as organic light emitting diodes (OLEDs). Firstly, developments with sample rotation, oxygen flooding and low energy sputtering are shown to improve depth resolution on thin GaSb/InAs/GaSb multilayers. Secondly, protocols using caesium sputtering were developed to characterise the water transmission rate in the barrier layers used to protect OLEDs.

SCIENTIFIC COLLABORATIONS: CNRS-LTM, Lyon University

Context and Challenges

TOF-SIMS depth profiling is a powerful technique for characterising the in-depth composition of thin film electronic devices. However, the choice of ion beam and sputtering conditions must be adapted when new materials are considered to prevent damage or roughening of the material.

Main Results

Firstly, developments to improve the depth resolution of TOF-SIMS depth profiles for inorganic layers are shown on a III-V hetero-structure (Fig. 1). The use of ultra-low beam energy, oxygen partial pressure in the analysis chamber and sample rotation were found to improve depth resolution [1].

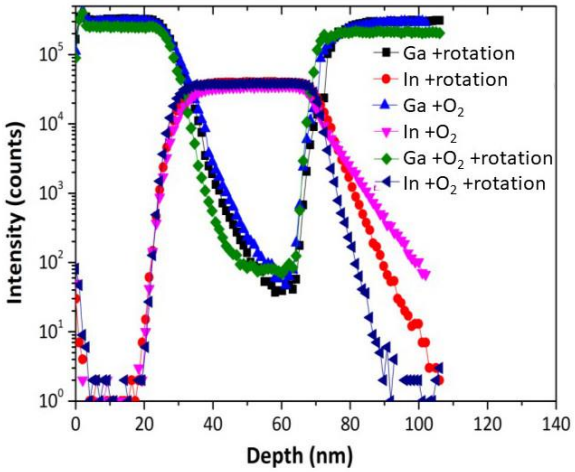


Figure 1: Ga and In TOF-SIMS depths profiles of a GaSb/InAs/GaSb multilayer performed at 250 eV impact energy, with sample rotation and oxygen flooding in the analysis chamber.

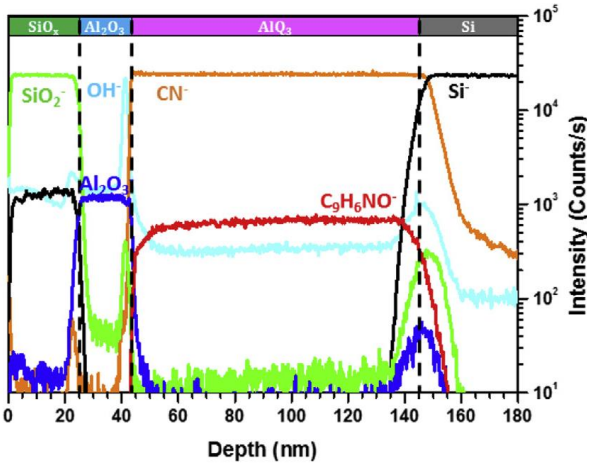


Figure 2: TOF-SIMS Cs^+ ion depth profile of an AlQ_3 layer that is capped with Al_2O_3 and SiO_2 to protect it from humidity.

Secondly, protocols to depth profile hybrid thin film structures found in OLED devices were developed. To observe the ingress of water molecules, using the OH^- secondary ion signal, into the protective cap a caesium ion beam was used (Fig. 2). The different layers are identified but there is limited molecular information in the AlQ_3 layer ($C_9H_6NO^-$ ion). To assess the molecular degradation in this layer an argon cluster beam was used, this greatly reduces ion beam induced fragmentation so that any loss in molecular ion intensity must come from a degradation of the sample [2].

Perspectives

Wedge crater preparation procedures are being developed to allow analysis of the same section by multiple techniques. Spectrometers with higher mass resolution and use tandem mass spectrometry will help improve peak ID and separation.

RELATED PUBLICATIONS:
[1] G. Beainy et al., Scripta Materialia, 2018, https://doi.org/10.1016/j.apsusc.2018.02.009
[2] T Terlier et al., Organic Electronics, 2018, https://doi.org/10.1016/j.orgel.2018.04.031

Advanced X-Ray Characterisation: Application to Thin Films for Memory Devices

RESEARCH TOPIC:

PCRAM, CBRAM, chalcogenides, phase change, x-ray diffraction, x-ray reflectivity, x-ray fluorescence, stress, strain

AUTHORS:

F. Fillot, W. Pessoa, E. Nolot, P. Noé, C. Sabbione, (F. Hippert), (D. Eichert)

ABSTRACT:

Advanced X-ray characterization strategies are being developed in order to address the need for accurate analysis of thin chalcogenide materials for memory applications. First, we present the evaluation of Phase Change Material (PCM) thin films by concomitant, complementary and combined in-situ X-ray diffraction (XRD) and X-ray reflectivity (XRR) techniques. Combined in-situ X-ray scattering techniques demonstrates the possibility to investigate with accuracy the structural, morphological and mechanical variations occurring in the films upon crystallization. Secondly, we show that the combination of X-ray reflectivity (XRR) and X-ray fluorescence (GIXRF) in glancing incidence geometry permits non-destructive chemical depth-profiling analysis in thin chalcogenide stacks with composition-driven properties.

SCIENTIFIC COLLABORATIONS : Grenoble INP, CNRS-LTM, ELETTRA Synchrotron

Context and Challenges

Recently, telluride materials (such as GeSbTe, SbTe, TiTe, etc.) have received an increased interest for Resistive Random Access Memories (RRAM), such as Phase Change Random Access Memory (PCRAM) and Current Bridging Random Access Memory (CBRAM), some of most promising candidates for the next generation of non-volatile memories.

Main Results

The thermal crystallization process of $Ge_2Sb_2Te_5$ (figure 1) is correlated to a volume shrinkage [1] (densification and thickness reduction) and to structural change with a tensile strain build-up. The combined XRD/XRR analysis gives new insights into the stress components built up in phase change material [2]. Afterwards, concomitant grain growth, viscous flow, densification and thickness accommodation are observed which leads to a partial stress relaxation in the PCM films. This combination of X-ray characterization techniques proposes a new approach in order to go further in the understanding of the phase change involved. This methodology is applied also on nitrogen-doped $Ge_2Sb_2Te_5$ samples [1].

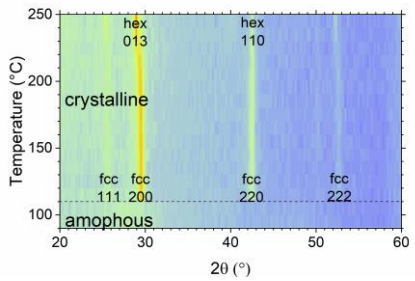


Figure 1: X-ray diffraction patterns (θ-2θ) of a 100 nm thick GST film as a function of temperature during a temperature profile.

The combination of X-ray reflectivity and X-ray fluorescence in glancing incidence geometry (XRR-GIXRF) was used both in the lab and at the synchrotron to reveal process-induced modification in ultrathin amorphous titanium telluride layers grown by physical vapor deposition (PVD) and capped in-situ with tantalum [3]. After careful metrology of the GIXRF-XRR instrumental function, the targeted depth-dependent Ti:Te ratio and the undesired diffusion of tantalum cap into the TiTe layer were unambiguously revealed. This was subsequently confirmed by plasma-profiling time-of-flight mass spectrometry (PP-TOFMS) and X-ray photoemission spectroscopy. Although improvement in the data reduction software is still needed in order to parametrize in-depth elemental distribution, this result already demonstrates how appropriate GIXRF/XRR technique can be as an almost "fab-ready" non-destructive depth-profiling technique for complex thin materials with composition-driven properties [3].

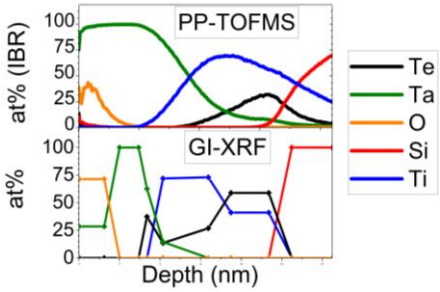


Figure 2: Chemical depth-profile of a 10 nm-thick TiTe layer capped in-situ with 5 nm of tantalum.

During the PVD process, the Ti:Te ratio was tuned so as to get a Ti-rich top layer and a Te-rich interfacial layer. GIXRF-XRR deduced profiles (figure 2) are compared with destructive mass spectrometry analysis (PP-TOFMS).

Perspectives

The structural and mechanical state at the nano-scale is under investigation by X-ray scattering. Macro-scale vs. nano-scale stress built-up upon crystallisation will be dissociated and correlated.

RELATED PUBLICATIONS:

[1] F. Fillot et al J. of Appl. Cryst., 2018, https://doi.org/10.1107/S1600576718015315

[2] P. Noé et al, Semicond Sci. Tech., 2018, https://doi.org/10.1088/1361-6641/aa7c25

[3] W. Pessoa et al, Spectrochimica Acta Part B: Atomic Spectroscopy, 2018, https://doi.org/10.1016/j.sab.2018.07.003

High Spatial Resolution Kelvin Force Microscopy: Application to Nanostructured and Photoactive Materials

RESEARCH TOPIC:
Work function, photocarrier dynamics

AUTHORS:
Łukasz Borowik, Pablo A. Fernandez Garrillo, (P. Roca i Cabarrocas, Benjamin Grévin),

ABSTRACT:
This protocol allows the local investigation of absolute work function and photo-carrier dynamics values over nanostructured samples. It can be implemented in electronic structures and device characterization as demonstrated here on HOPG sample or over the cross-sectional profile of crystalline and epitaxial silicon. Additionally, the results can be analyzed by the numerical simulation routine that enables to compare simulations and experimental results.
In future work we will focus on the photo-voltage interpretation as a function of the illumination wavelength and propose an acquisition setup to measure minority carrier diffusion length at the nanoscale.

SCIENTIFIC COLLABORATIONS : CNRS INAC SYMNES, Ecole Polytechnique

Context and Challenges
Kelvin probe force microscopy (KPFM) provides spatially resolved measurements of the surface potential, i.e. relative to the sample surface work function (WF), which is a parameter of utmost importance in the description and control of any electronic device behavior as well as charge carrier injection and transport. Moreover, surface potential measured under frequency-modulated illumination can be used to probe photo-carrier dynamics that play equally important roles in photovoltaic and electroluminescent devices.

Main Results
We propose and demonstrate a protocol to acquire absolute spatially resolved WF measurements. Different monocrystalline metallic (Ag, Cu, Al) reference samples were firstly used for the KPFM WF tip calibration. Afterwards, the absolute WF value was measured on ZYB grade HOPG sample (Fig. 1).

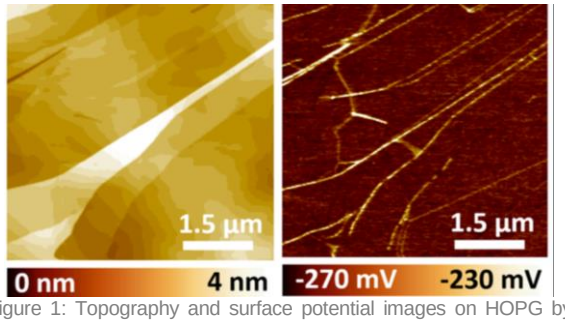


Figure 1: Topography and surface potential images on HOPG by KPFM.

The calibrated HOPG WF value is equal to 4.6 ± 0.03 eV, corresponding to -260 mV of surface potential on HOPG flakes [1] which agrees with the HOPG theoretical value.
Furthermore, we demonstrate KPFM combined with frequency modulated illumination excitation to probe photocarrier dynamics over the cross-section of an epitaxial silicon solar cell.

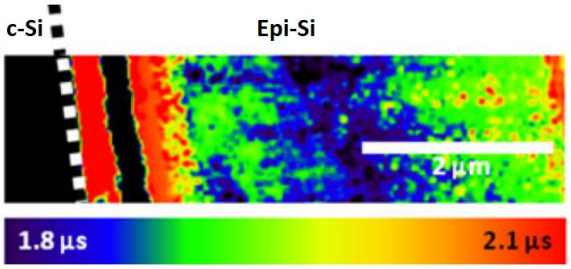


Figure 2: Cross-sectional profile of crystalline and epitaxial silicon showing the photo-voltage decay time, attributed to the effective minority carrier lifetime of free carriers in the sample.

In this work we map two carrier recombination processes on the cross-sectional profile: 1) an effective minority carrier lifetime, and 2) a longer SPV decay time constant attributed to the trapping de-trapping effect, common in silicon (Fig. 2). [2]
Additionally, we propose an automatic numerical simulation routine that enables to predict the behavior of spectroscopy curves of the average surface photovoltage as a function of a frequency-modulated excitation source, enabling the comparison of simulations and experimental results. We compare this simulation routine against experimental results previously obtained on a silicon nanocrystal solar cell, as well as on a polymer/fullerene bulk heterojunction device. [3]

Perspectives
The relationship between the surface potential – measured as a function of illumination wavelength – and the minority carrier diffusion length is well known. In future work, we will focus on the photovoltage interpretation as a function of the illumination wavelength and propose an acquisition setup for measuring the minority carrier diffusion length at the nanoscale.

RELATED PUBLICATIONS:
[1] Fernandez Garrillo P.A. et al., Rev Sci. Instrum. 2018, http://dx.doi.org/10.1063/1.5007619
[2] Fernandez Garrillo P.A. et al., IEEE J. Photovolt. 2018, http://dx.doi.org/ 10.1109/JPHOTOV.2018.2793760
[3] Fernandez Garrillo P.A. et al., BJNano, 2018, http://dx.doi.org/10.3762/bjnano.9.175

Multi-Technique Approaches to 3D Imaging

RESEARCH TOPIC:
Multiscale correlative nanocharacterization, 3D analysis, spectroscopy.

AUTHORS:
Z. Saghi, J. Sorel, M. Jacob, N. Bernier, J.P. Barnes, M. Moreno, N. Chevalier, (B. Gautier, F.Bassani, T. Sanders, J. Rodriguez-Viejo)

ABSTRACT:
The 3D complexity of modern nanodevices necessitates the application of several imaging and spectroscopy techniques. The Nanocaracterization Platform offers an ideal environment for 3D correlative studies at different length scales and resolutions. In this work, we show how TOF-SIMS and AFM can be combined to provide accurate 3D chemical composition of a GaAs/SiO_2 heterostructure, by taking into account the sample topography. At a smaller scale, we highlight the complementarity of HAADF-STEM tomography and EDX-STEM tomography for a comprehensive morphological and chemical analysis of an As-doped silicon fin-shaped structure.

SCIENTIFIC COLLABORATIONS: INSA Lyon, INAC, LTM-CNRS, Arizona State University, Barcelona University.

Context and Challenges
The complex, heterogeneous architectures of modern devices require accurate 3D characterization at many length scales. The combination of characterization techniques that produce reliable morphological information with ones that supply compositional information is increasingly important to reduce measurement artefacts and obtain a reliable 3D data set. Examples of this approach include combining time-of-flight secondary ion mass spectrometry (TOF-SIMS) with atomic force microscopy (AFM), transmission electron microscopy (TEM) with atom probe tomography, and electron tomography in imaging and spectroscopy modes.

Main Results
3D TOF-SIMS analysis provides high sensitivity analysis of the composition of semiconductor structures. However, when analysing heterogenous samples, the initial topography and the difference in erosion rates of the different materials present may distort the final 3D volume. We have developed a protocol that uses AFM imaging at each horizontal interface in the sample to be able to correct the 3D volume [1]. An example on a GaAs/SiO_2 heterostructure is shown in Fig. 1.

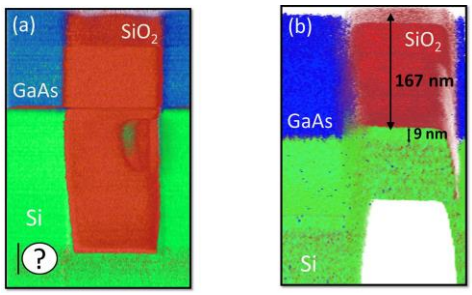


Figure 1: TOF-SIMS data set (a) before and (b) after correction using AFM and profilometer data.

High angle annular dark field scanning TEM (HAADF-STEM) tomography enables the morphological study of complex 3D nanostructures, with a nanometre resolution [2]. Combining this technique with spectroscopy modes such as electron energy loss spectroscopy (EELS) or energy dispersive X-ray analysis (EDX) is of great interest for the semiconductor industry. We have put in place machine learning techniques and reconstruction algorithms adapted for these modes. Fig. 2 shows an example of HAADF-STEM (left) and EDX-STEM (right) tomography applied to an As-doped silicon fin-shaped structure [3]. From the reconstructed volumes, it was possible to estimate the roughness of the Si structure, the dopant implantation depth and the mean size of the As precipitates.

	HAADF-STEM	EDX-STEM
RMS roughness	3nm	No
Mean cluster size	≃ 15 nm³	≃ 20 nm³
Implantation depth	No	≃ 20nm

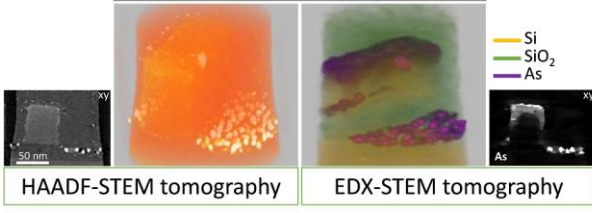


Figure 2: 3D morphological and elemental analysis of an As-doped Si structure by correlative HAADF-STEM and EDX-STEM tomography [3].

Perspectives
Multiscale correlative nanocharacterization approaches to support device development will continue on two aspects. Firstly, the development of experimental protocols to combine techniques, including the use of protected environment transfer systems and the correlation of electrical properties with composition. Secondly, the use of advanced algorithms and machine learning tools for multi-technique *quantitative* analysis.

RELATED PUBLICATIONS:
[1] M. Moreno et al., JVST B, 2018, https://doi.org/10.1116/1.5019464
[2] P. Ferrando-Villalba et al., Sci. Rep., 2018, https://doi.org/10.1038/s41598-018-30223
[3] J. Sorel et al., Microsc. Microanal., 2018, https://doi.org/10.1017/S143192761800243X

Correlation of Cathodoluminescence and (S)TEM for Defects Analysis in III-V Material

RESEARCH TOPIC:
III-V, heteroepitaxy, cathodoluminescence, STEM

AUTHORS:
J.Roque, N.Rochat, (S. David)

ABSTRACT:
InGaAs quantum wells (QW) embedded in (Al)GaAs barriers and grown on (001) silicon substrates by metalorganic chemical vapor deposition are studied. An appropriate method combining cathodoluminescence and (scanning) transmission electron microscopy characterization is performed to spatially correlate the optical and structural properties of the QW. The combined interpretation of luminescence and TEM measurement provides an exhaustive landscape of such complex samples allowing a deep understanding on the impact of particular defect or structure morphology (composition, strain) on the optoelectronic characteristics.

SCIENTIFIC COLLABORATIONS : CNRS/LTM

Context and Challenges
III-V semiconductors are widely recognized as an opportunity to improve the micro- and nanoelectronic integrated circuit capabilities and could allow the development of low consumption and high-frequency devices or optoelectronic devices. Development of these applications requires co-integration of III-V with silicon technology. Heteroepitaxy of III-V material on silicon can result in numerous structural defects that can dramatically affect the performances of components. In order to improve the quality of III-V material on silicon, spatial correlation of cathodoluminescence (CL) and scanning transmission electron microscopy (STEM) is use to understand impact of morphology or defects on optoelectronic properties.

Main Results
An appropriate method combining CL and high resolution (HR) STEM characterization is performed to spatially correlate the optical and structural properties of InGaAs/(Al)GaAs QW structure. Full blanket QW have been characterized.

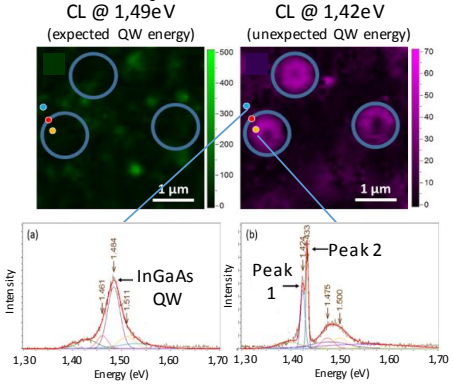


Figure 1: Blanket QW CL intensity mapping at 1.49 eV and 1.42 eV. Regions shown by blue and yellow dots exhibit different CL spectrum shown below in (a) and (b).

These samples, as expected for heteroepitaxy growth, exhibit strong inhomogeneities across the surface due to the high density of defects. Moreover, unexpected very localized luminescence energy, regarding the expected QW structure, is detected (Fig. 1). Thanks to correlation, these features have been related to areas with a local enrichment of C in the barrier and of In in the QW probably due to a particular barrier strain state. These observations are coherent with the low energy luminescent doublet circular feature observed on the sample.
This method has been also applied to aspect ratio trapping growth (Fig. 2). In this case, we observe the appearance of a chemical ordering in the InGaAs QW. This has been related to a low intensity emission and a lower energy of the QW. We demonstrate that the disappearance of this ordering by annealing increase by 2 orders of magnitude the QW intensity emission and helps to recover the expected QW energy.

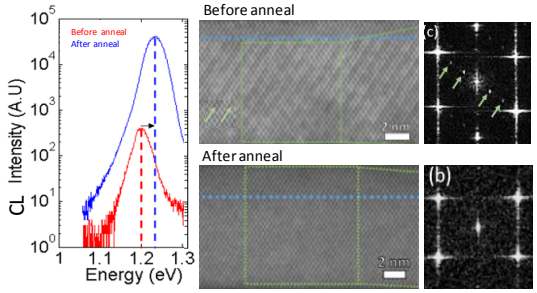


Figure 2: CL spectrum before and after annealing and respective HRSTEM images and Fourier transform showing chemical ordering.

Perspectives
The results obtained on these two different QW structures illustrate the power of CL and STEM correlation. The method, although complex and time consuming, allows a full understanding of the complex phenomenon occurring with heteroepitaxy. This method will be now applied to In(Al)GaN/GaN QW structures.

RELATED PUBLICATIONS :
[1] J. Roque et al, Journal of Vacuum Science & Technology B 36, 042901 (2018), https://doi.org/10.1116/1.5033363
[2] J. Roque et al, Applied Physic Letter. 112, 202104 (2018). https://doi.org/10.1063/1.5027163

Probing Critical Buried Interfaces with Hard X-Ray Photoemission

RESEARCH TOPIC:

Nano-Characterization, surface and interface analysis, buried Interfaces.

AUTHORS:

O. Renault, E. Martinez, C. Zborowski, M. Kazar Mendes, A. Torres, M. Bernard, R. Gassilloud, N. Barrett (J. M. Ablett, J. P. Rueff, Y. Yamashita)

ABSTRACT:

Hard X-ray photoelectron spectroscopy (HAXPES) enhances the capabilities of conventional X-ray photoelectron spectroscopy (XPS) due to a larger probing depth. This enables the non-destructive analysis of critical interfaces in device structures that were otherwise inaccessible due to the limited depth sensitivity of XPS. Here, some results illustrating the new opportunities of using HAXPES for surface and interface analysis in device technology are presented, addressing cases where critical interfaces are either moderately (15 nm) or deeply buried (50 nm) below the surface.

SCIENTIFIC COLLABORATIONS: University of Southern Denmark, CEA-IRAMIS/SPEC, Synchrotron SOLEIL, National Institute of Materials Science (NIMS, Japan), Institute of Nanotechnology in Lyon (INL).

Context and Challenges

The microelectronic industry needs advanced characterization to manufacture complex devices with tailored properties critically controlled by the quality of buried interfaces. Hard X-ray photoelectron spectroscopy (HAXPES) allows a non-destructive chemical analysis of these buried interfaces (25 nm) using core-level spectra. When combined with inelastic background analysis, HAXPES can analyze quantitatively elements deeply buried below a < 70 nm-thick overlayer.

Main Results

HAXPES was first implemented in GaN-based HEMT devices to study the integrity of the AlGaN channel below thick Al/Ta source/drain metal contacts (Fig. 1). It is demonstrated that by exploiting the inelastic background in the spectrum, it is possible to determine within a 10% accuracy and below the distribution of elements over large depths (< 70 nm), thereby enabling to follow diffusion phenomena at interfaces [1,2].

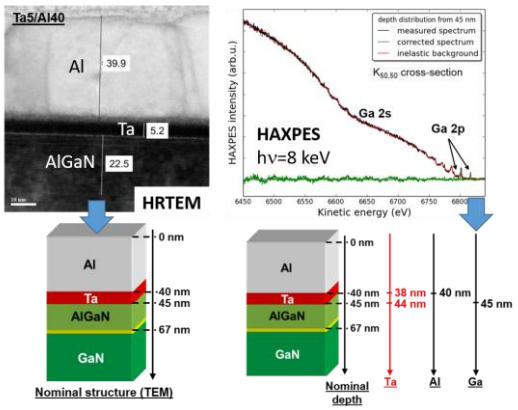


Figure 1: HAXPES of deeply buried interfaces in HEMT devices and elemental depth distribution using inelastic background analysis.

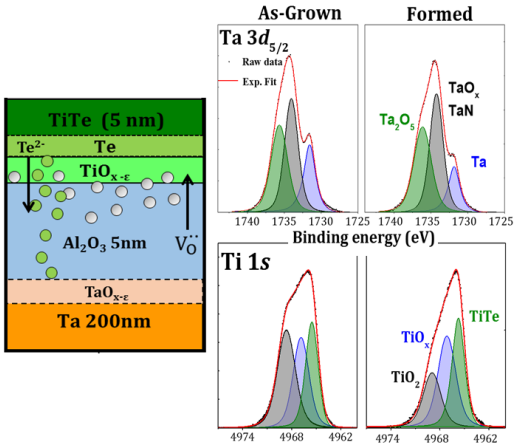


Figure 2: HAXPES analysis of buried interfaces in TiTe/Al_2O_3 conductive-bridge resistive memories (CBRAM).

HAXPES was also performed on CBRAMs structures at the SOLEIL synchrotron (Fig. 2) to investigate the critical interfaces between the electrolyte (Al_2O_3) and the TiTe top and Ta bottom electrodes. During resistive switching, the TiOx layer at the TiTe/Al_2O_3 top interface is reduced and the TaOx at the Al_2O_3/Ta bottom interface is oxidized. These interfacial redox processes are related to an oxygen drift across the electrolyte under the applied bias [3].

Perspectives

HAXPES has proven to be a very powerful technique to probe critical buried interfaces in device structures but is still mostly implemented at synchrotron radiation facilities. Laboratory HAXPES is rapidly emerging, opening novel perspectives for routine analysis [4]. However, an extensive use of this technique for thin films applications will require work on quantification and data treatment.

RELATED PUBLICATIONS:

[1] C. Zborowski et al., Appl. Surf. Sci.**432** (2018) https://doi.org/10.1016/j.apsusc.2017.06.081
[2] C. Zborowski et al, J. Appl. Phys. **124**, (2018) https://doi.org/10.1063/1.5033453
[3] M. Kazar Mendes et al., Scientific Reports 8 (2018) https://doi.org/10.1063/1.5033453
[4] O. Renault et al., Surf. Interface Anal. 2018; https://doi.org/10.1002/sia.6451

Advanced Microscopic Characterization of the Electronic Properties of 2D Materials

RESEARCH TOPIC:
2D materials, nano-characterization

AUTHORS:
O. Renault, M. Gay,T. Dau, (M. Jamet, H. Kim, A. Kis)

ABSTRACT:
The rising field of two-dimensional (2D) materials beyond graphene such as transition-metal dichalcogenides (TMDC) opens new opportunities in device technology towards sustainability of the materials supply chain. A key component is the qualification of materials and processes and the study of prototypical devices. It becomes a challenging task to characterize in a suitable, reliable and efficient way the electronic properties of these new materials and address the issue of processing-dependent properties. Here, we show how photoemission electron microscopy in momentum space (*k*PEEM) can tackle this challenge in the case of $MoSe_2$-based heterostructures.

SCIENTIFIC COLLABORATIONS: Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland), CEA-IRIG/SP2M, INAC, Institut Néel.

Context and Challenges
2D material heterostructures are being considered as a potential route towards scaling of future devices. Yet, to the end of both process optimization and test devices qualification, suitable characterization techniques are essential for a microscopic analysis of the novel electronic properties of 2D materials. Here, applications of an efficient laboratory tool, photoemission momentum microscopy (kPEEM) are presented.

Main Results
A first result deals with $MoSe_2$/graphene heterostructures grown by van der Walls epitaxy, a growth technique compatible with large area deposition [1]. Fig. 1 presents the band structure of the material, depicting the energy dispersion according to momentum of the valence electrons. Such a plot enables to retrieve the electronic properties of the atomically-thin MoSe2 and a 250 meV band gap opening in the underlying graphene arising from interface charge transfer and concomittant electronic depletion in the graphene.

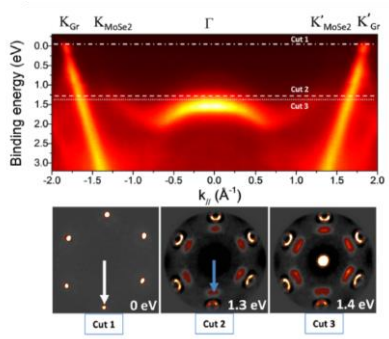


Figure 1: Band structure of MoSe2/graphene heterostructure by kPEEM. Cut1 is the momentum map of graphene close to Fermi level; Cut2, 3 are MoSe2 maps at the K and Γ point respectively.

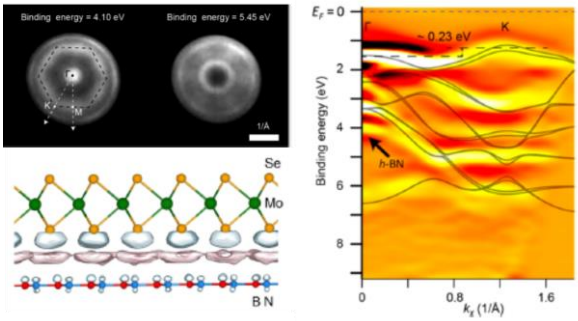


Figure 2 : Band structure of MoSe2/h-BN/Rh(111) heterostructure by kPEEM and DFT calculation of the electron density.

Fig. 2 shows the band structure analysis of another $MoSe_2$ heterostructure, first revealing directly the monolayer character of the $MoSe_2$ with the valence band maximum being at the K point, 0.23 eV closer to the Fermi level than the Γ point. Besides, further analysis shows that the band structure of $MoSe_2$ resembles that of the free-standing counterpart, thereby showing that the electronic properties of the original material are preserved in the heterostructure. A curvature analysis of the bands provides a direct measure of the hole effective mass in the material, while the characteristic reciprocal distance is directly related to the in-plane lattice constant, otherwise difficult to retrieve from X-ray diffraction.

Perspectives
*k*PEEM is a valuable tool for a direct and reliable characterization of the electronics of 2D materials and heterostructures at the micron-scale. It is anticipated that the use of this technique will grow and be complemented by operando measurements.

RELATED PUBLICATIONS :
[1] T. Dau et al., *ACS Nano* **12**, (2018). https://doi.org/10.1021/acsnano.7b07446
[2] M. Chen., *NPJ 2D Materials and Applications* **2**, (2018). https://doi.org/10.1038/s41699-017-0047-x
[3] M. Chen, *ACS Nano* 12 (2018). https://doi.org/10.1021/acsnano.8b05628

In Depth Analysis of Molecular Cross-Contamination in FOUPs

RESEARCH TOPIC:

FOUP polymer, Airborne Molecular Contamination (AMC), HCl, HF, diffusivity, solubility, adsorption, Cu surface, gas purge.

AUTHORS:

H. Fontaine, M-P. Tran, (P. Gonzalez-Aguirre), C. Beitia, (S-I. Moon, J. Lundgren)

ABSTRACT:

Molecular contamination mechanisms of polymers used for FOUPs were determined for HCl, leading to the determination of solubility and diffusivity coefficients in PC, EBM and EBM/CNT materials. Then, a linear model of HCl deposition on Cu surfaces was established depending on time and HCl airborne concentration whatever the relative humidity (0% up to 70%). Such basic knowledge allows both to evaluate the FOUP capacity to sorb and outgas HCl but also to assess the level of HCl transferred on Cu-stored coated-wafers. Also, FOUP decontamination and contamination control solutions were evaluated for HF, showing that wet cleaning process has a low efficiency whereas clean gas purge significantly limits contamination transfer to stored wafers.

SCIENTIFIC COLLABORATIONS: Entegris-Leti common lab

Context and Challenges

FOUP to wafer acidic molecular contamination (HF, HCl…) can be highly detrimental leading to defectivity and yield losses in microelectronic manufacturing (e.g. Cu & Al corrosion). Such issues are due to the capacity of FOUP polymers to sorb but also to subsequently outgas and transfer molecules to stored wafers. These phenomena are governed by solubility and diffusion of contaminants in polymer as well as their deposition affinity on the wafer. The knowledge of basic mechanisms such as FOUP decontamination is key to control contamination risks and implement containment solutions. Thus, HCl contamination mechanisms were studied as well as purge gas and wet cleaning processes to decontaminate FOUPs.

Main Results

HCl sorption kinetics determined in FOUPs polymers have showed that basic mechanisms are in agreement with a Fickian diffusion. Thus, HCl solubility (S) and diffusivity (D) were obtained in polycarbonate (PC), Entegris Barrier Material (EBM, a cycloolefin polymer) and even for EBM charged with Carbon NanoTubes (EBM/CNT) (Fig. 1) [1].

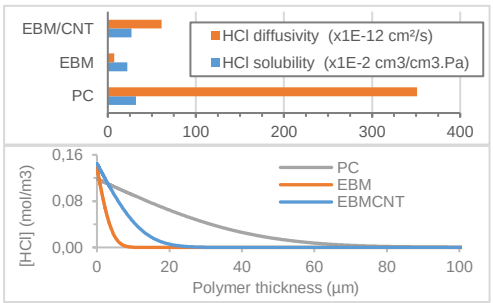


Figure 1: Solubility (S) and diffusivity (D) of HCl in PC, EBM and EBM/CNT (top) and their application to define the [HCl] profile in a FOUP polymer membrane by numerical simulation (Comsol Multiphysics), HCl exposure to 800ppbV during 2h (bottom).

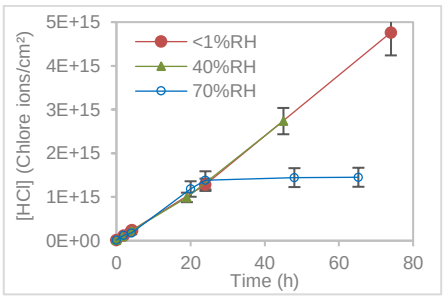


Figure 2: HCl deposition kinetics on Cu for different levels of relative humidity.

Solubility is very low and relatively similar whatever the material. EBM and EBM/CNT materials present a much lower diffusivity than PC characterizing their better potential to avoid HCl sorption as highlighted by numerical simulation (Fig. 1).

On the other hand, a linear model of HCl deposition on Cu surfaces was established depending on time and HCl airborne concentration whatever the relative humidity (0% up to 70%) and up to the contaminant monolayer (~10^{+15} Cl atoms /cm²) [2]. Beyond this threshold value, Cu corrosion occurs and HCl deposition happens differently depending on moisture.

Finally, FOUP decontamination and contamination control solutions were also studied in the case of HF, showing respectively, that wet clean process has a low efficiency whereas a clean gas purge strongly limits contamination transfer to wafers.

Perspectives

The characterization of FOUP polymers contamination mechanisms is currently pursued both in case of other critical molecules and for current and new FOUP polymers including composites. In addition, intentional contamination studies of FOUPs will be carried out to validate expected FOUP behavior with respect to the mechanisms determined in this work.

RELATED PUBLICATIONS:

[1] M-P. Tran et al., Solid State Phenomena, 2018, https://doi.org/10.4028/www.scientific.net/SSP.282.321
[2] M-P. Tran et al., SPCC conference, 2018, https://linxconferences.com/wp-content/uploads/2018/04/02-08-MP_Tran.pdf
[3] P. Gonzalez-Aguirre et al., Microelectronic Engineering, 2018, https://doi.org/10.1016/j.mee.2018.03.002

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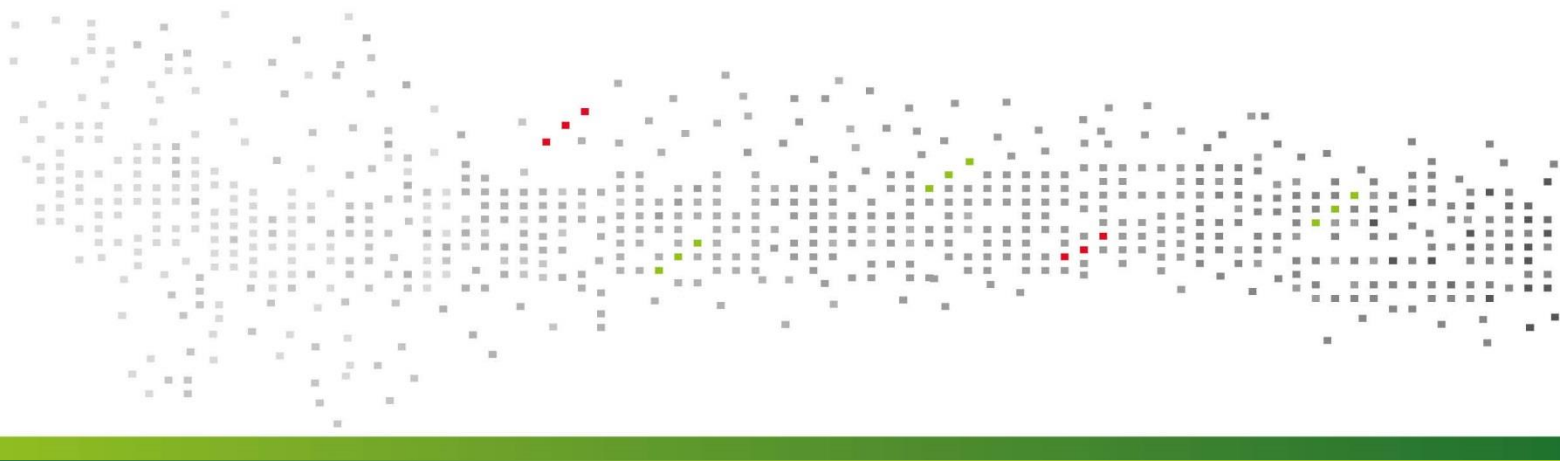

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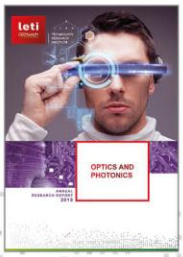

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