cea leti

3D integration for HPC & AI

Active interposer technologies for advanced chiplet-based systems: CMOS to photonic and quantum architectures

What is an Active Interposer?

The chiplet-on-interposer concept involves integrating a multiplicity of chips on a common Silicon platform unlike the concept of large monolithic systems on chip (SoCs).

The active interposer extends this notion by adding smart functions at interposer level, in particular by integrating CMOS components. The interposer is more than a simple interconnection platform; it becomes the foundation for analog and low power digital and photonic functions and increased 3D communication, especially with network-on-chip architectures.

Applications

High performance computing & artificial intelligence:

- Big Data
- Deep learning
- Cryptanalyze & Crypto money
- Physical simulation
- Climate model
- Astrophysics

Embedded computing:

- Edge AI
- Aeronautics
- Automotive
- Internet of Things

Work performed in the frame of the IRT Nanoelec consortium.

NANOELEC.

What's new?

Active interposer architecture offers multiple advantages:

Architecture agility through partitioning:

- Large single die divided in a multitude of smaller dice ensuring lower advanced node costs
- Highly configurable, optimized chiplets based on generic computing cores, GPU, FPGA fabric, AI accelerators, advanced memories, etc.
- Analog functions economically moved to interposer in a relaxed CMOS node; I/O services can be included

Performance breakthrough compatible with mass production:

- Power efficiency through embedded DC/DC converters
- 3D links for high performance with modern communication protocols and network-on-chip architectures
- Manufacturing and packaging demonstrated on 300 mm CMOS platform

Results

The INTACT proof of concept uses 96-core architecture comprising 6 chiplets (FDSOI 28 nm node) 3D-stacked on an active silicon interposer (CMOS 65 nm node).

- **Advanced 3D Technology**: 150,000 chiplet connections using ultra fine pitch die-to-die interconnect, 14,000 TSVs through interposer
- **Advanced 3D Architecture**: active interposer providing network-on-chip for chiplet-to-chiplet communication in a scalable, configurable, cache coherent system

CEA Leti's results pave the way to future high efficiency systems for high performance computing.

What's next?

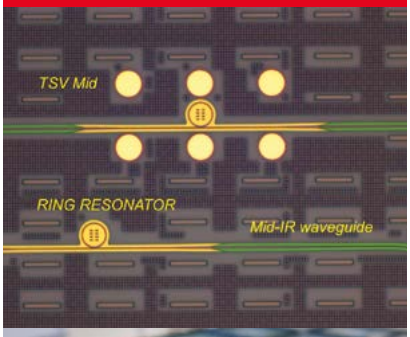
Pioneering mutation in advanced system integration:

- Active interposer to photonic interposer: Optical Network-on-Chip (ONoC), integrated wave guides and 3D technology
- 3D integration technological roadmap for density increase including High Density Through Silicon Vias TSV (Ø1 µm H10 µm) and hybrid bonding
- Quantum architecture key enabling cryo technologies

Main Publications

- P. Vivet et al., "A 220 Gops 96-core Processor with 6 Chiplets 3D-stacked on an Active Interposer offering 0.6 ns/mm Latency 3 TBit/s/mm² inter-Chiplet Interconnects and 156 mW/mm²@82% DC-DC Converters" ISSCC 2020

- P. Coudrain, et al., "Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures", ECTC 2019



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